A CAD Methodology for Optimizing Transistor Current and Sizing in Analog CMOS Design

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Current

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Transistor-level design methodology

- Design methodology
  - Select a circuit topology
  - Select desired performance specifications
  - Computerized optimization to select MOS currents and sizings to meet specs
  - Can also simulate topology over a range of currents and sizings and explore tradeoffs
- Transistor-level design methodology
  - Allows designer to pre-select near-optimal drain currents and sizings for any circuit
  - Considers transconductance g_m and output conductance g_{ds}
  - Permits design in weak, moderate, or strong inversion

MOS Inversion Coefficient

- Traditionally, degrees of design freedom are drain current I_D, channel width W and channel length L.
- Here, degrees of freedom are drain current I_D, channel length L and inversion level IC, which is a normalized measure of I_D describing level of channel inversion.

$$IC = \frac{I_D}{2n\mu C_{OX}(W/L)U_T^2}$$

$$n = (COX + VDEP)/COX,$$

$$U_T = kT/q$$

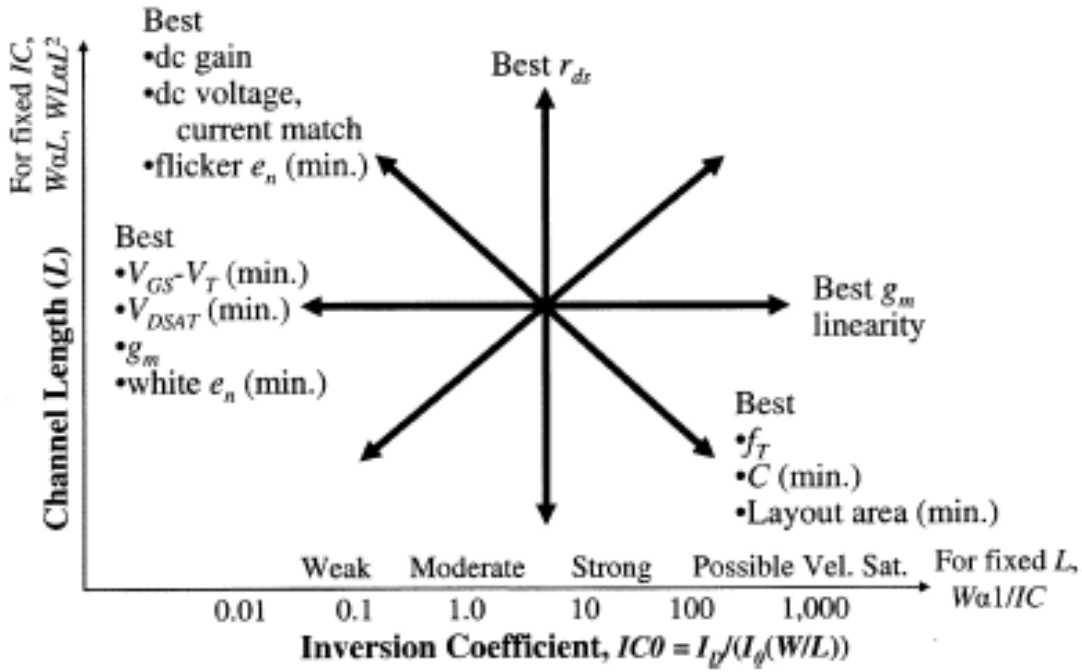
- Weak inversion: IC < 0.1 ($V_{GS} - V_T$ ~= -72mV)
  Moderate inversion center: IC = 1.0 ($V_{GS} - V_T$ ~= 40mV)
  Strong inversion: IC > 10 ($V_{GS} - V_T$ ~= 220mV)

Performance Tradeoffs – MOS Operating Plane

$$IC_0 = \frac{I_D}{2n_0\mu_0 C_{OX}(W/L)U_T^2} = \frac{I_D}{I_0(W/L)}$$

- Fix n0 at moderate inversion, mu0 at low field value.
- I0 is technology current

- Best C and intrinsic-gain bandwidth f_T at high IC, small L.
- Opposite for intrinsic gain, dc match, flicker noise.
- V_{DSAT}, g_m, white noise optimal at low IC.
- g_m linearity best at high IC

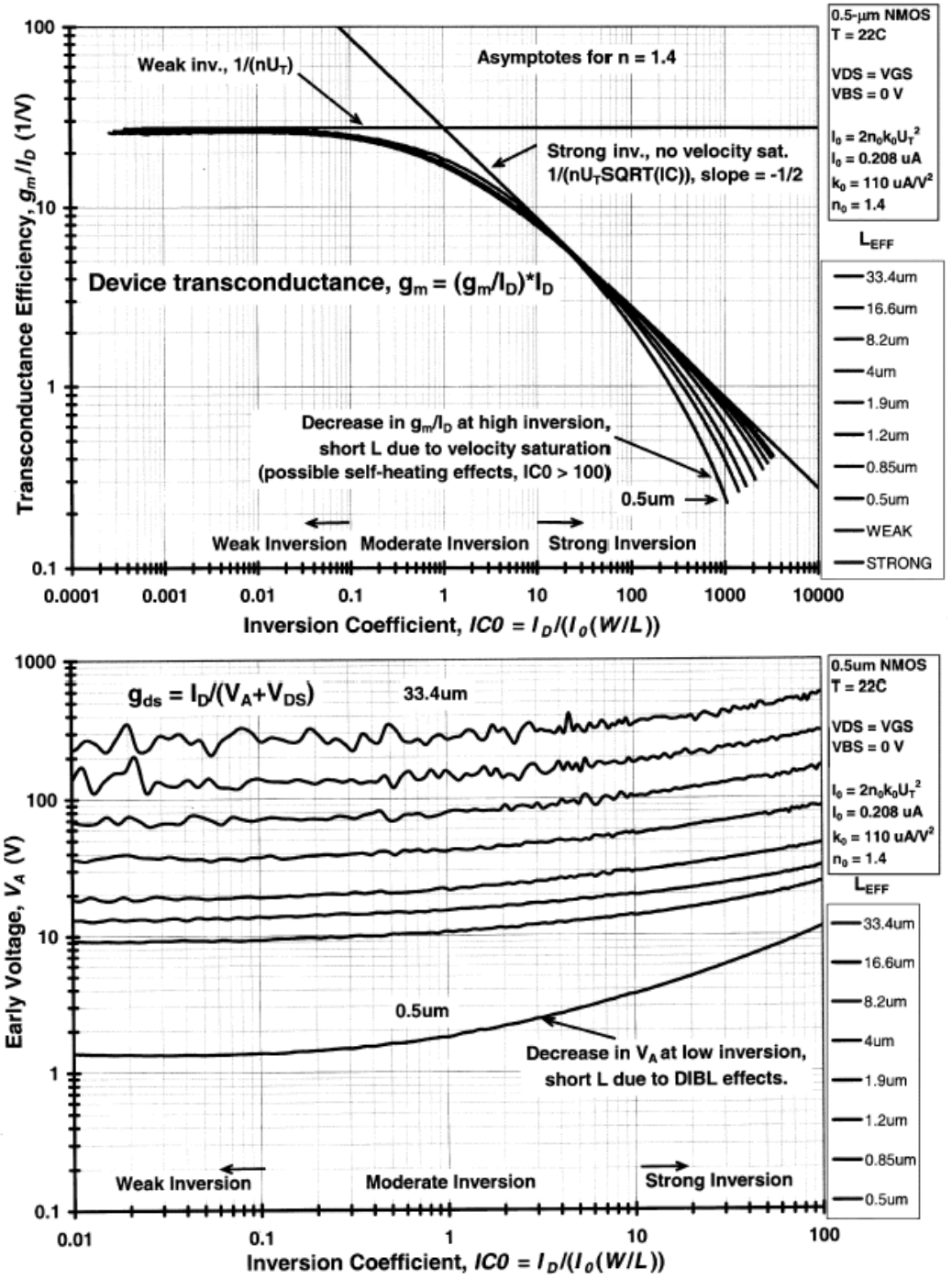


MOS Sizing Relationships

- If IC is increased (I_D and L fixed), (W/L) ratio, W, gate area (and C_{OX}), decrease inversely with increasing IC.
- If L is increased (I_D and IC fixed), W increases directly with L to maintain (W/L) ratio. Since W increases, gate area (and C_{OX}) increases as square of increasing L.
- If I_D increased (IC and L fixed), (W/L) ratio, W, and gate area (and C_{OX}) increase directly with increasing I_D.

MOS DC Bias Voltage and Small-Signal Parameter Relationships

- Weak/moderate inversion best for maximizing g_m and minimizing white noise
- Long channel length L results in higher V_A and subsequently lower output conductance g_{ds} → higher r_{ds}



Gain and Bandwidth

- Intrinsic gain is highest at weak inversion with long channel length L
- Intrinsic gain is lowest at strong inversion with short channel length L

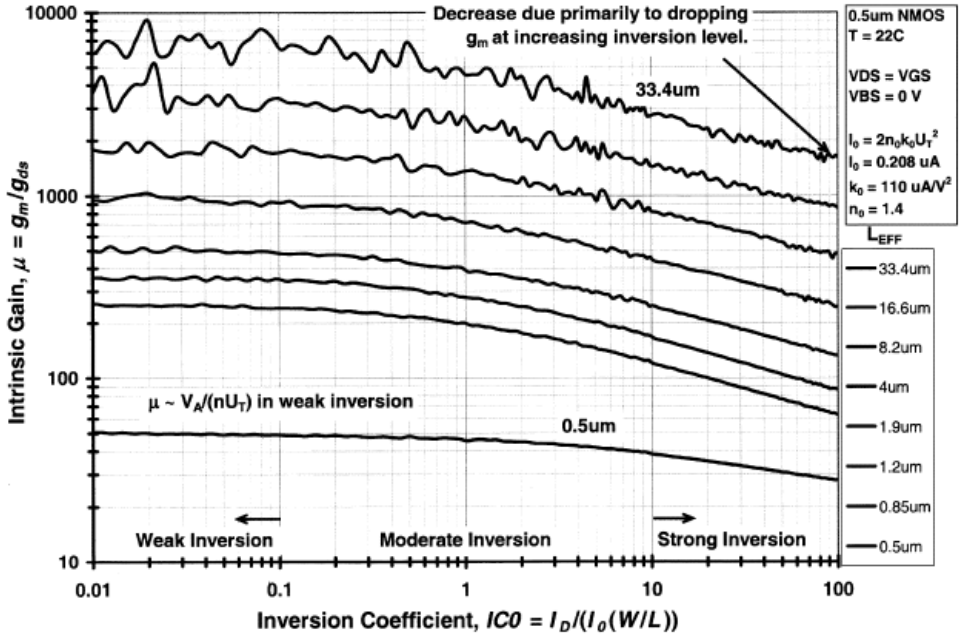
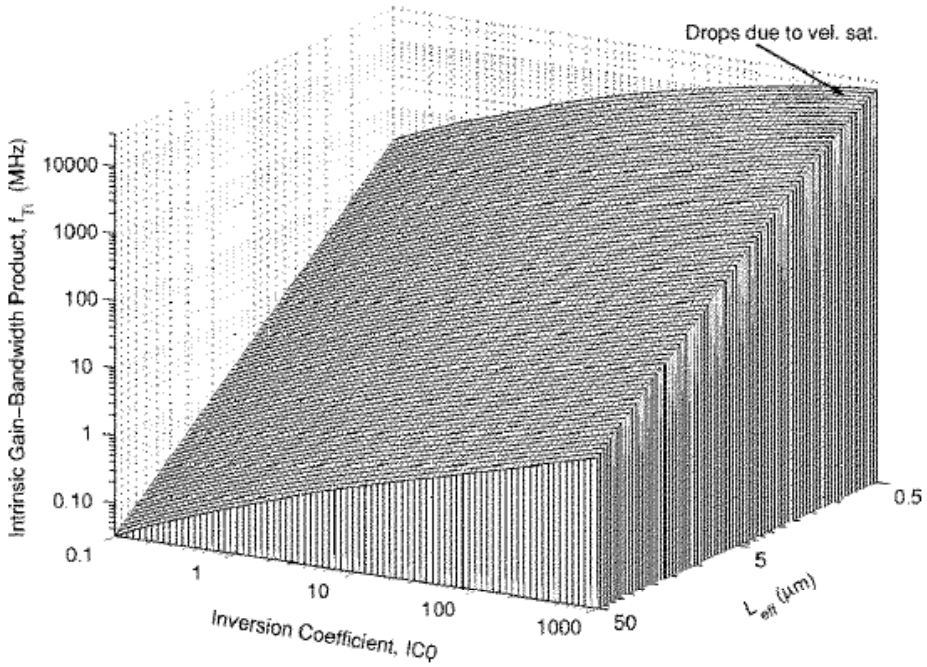


TABLE III
MOS GAIN AND BANDWIDTH RELATIONSHIPS

Parameter (W and L are effective dimensions.)	$IC_0 \uparrow$ L, I_D fixed	$L \uparrow$ IC_0, I_D fixed	$I_D \uparrow$ IC_0, L fixed
Intrinsic Gain[1,2]: $A_{V_i} = \frac{g_m}{g_{ds}} = \frac{I_D(g_m/I_D)}{I_D(g_{ds}/I_D)} = \frac{I_D/V_{gm}}{\approx I_D/V_A} \approx \frac{V_A}{V_{gm}} \approx \frac{VAL \cdot L}{nU_T\left(\sqrt{0.25+IC}+0.5\right)}$ (1)	Unchanged, W.I.[2] $\downarrow \propto \frac{1}{\sqrt{IC}}$, S.I.[1,2]	$\uparrow \propto L$[1,2]	Unchanged

Gain and Bandwidth cont'd

- Best BW at high IC0, short L
- Velocity saturation at high IC0, short L, causing BW to limit



Instrinsic Bandwidth[1]:

$$f_{Ti} = \frac{g_m}{2\pi\left(C_{gsi} + C_{gbi}\right)}$$

$$= \frac{\dfrac{IC_0}{\sqrt{0.25 + IC} + 0.5} \cdot \dfrac{I_0}{nU_T}}{2\pi\left(C'_{gsi} + C'_{gbi}\right)L^2 C_{OX}}$$

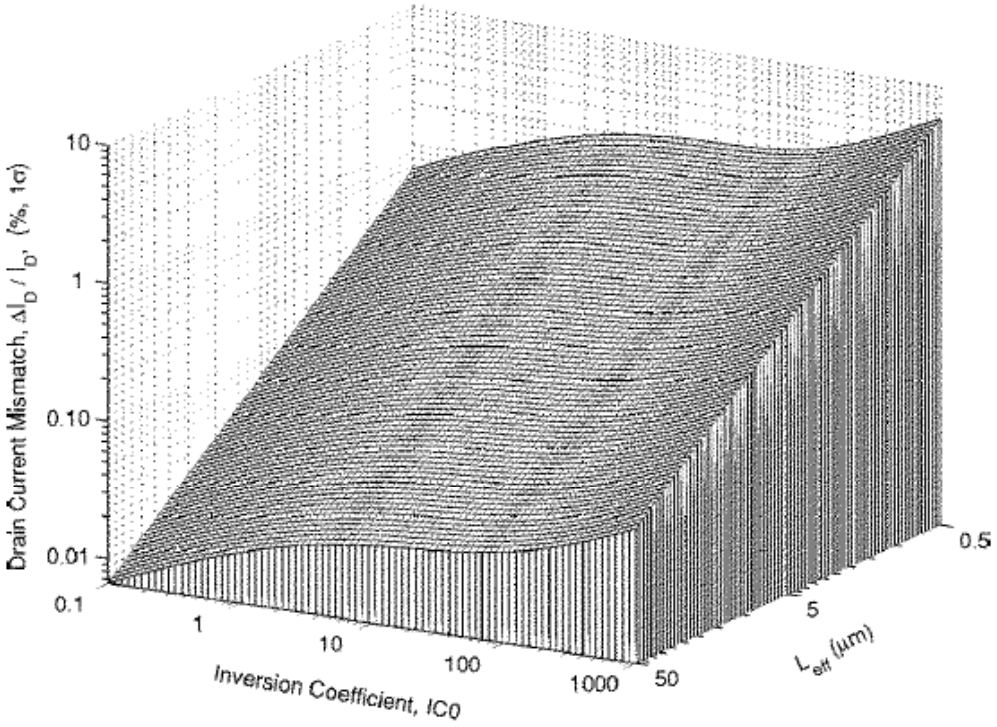
$\uparrow \propto IC$, W.I. $\uparrow \propto \sqrt{IC}$, S.I.[1]	$\downarrow \propto \frac{1}{L^2}$ [1]	Unchanged

$$C'_{gsi} = \frac{C_{gsi}}{WLC_{OX}} = \tfrac{0}{3}, \tfrac{1}{3}, \tfrac{2}{3}, \text{ for W.I., M.I., S.I.}$$

$$C'_{gbi} = \frac{C_{gbi}}{WLC_{OX}} = \left[\tfrac{3}{3}, \tfrac{2}{3}, \tfrac{1}{3}\right]\tfrac{n}{n-1}, \text{ for W.I., M.I., S.I}$$

DC Mismatch and Gate-Referred Flicker Noise

- Since mismatch dependant on I_D. Normalization of ID offset required for different ID
- I_D current mismatch optimized at long L, low IC.
- In strong inversion, ID mismatch almost independent of IC



Threshold Voltage Mismatch:

$$\Delta VTO = \frac{AVTO}{\sqrt{WL}} = \frac{\sqrt{IC_0}}{L}\sqrt{\frac{I_0}{I_D}}AVTO \qquad (1)$$

$\uparrow \propto \sqrt{IC_0}$

$(WL \propto \frac{1}{IC_0})$

Transconductance Efficiency[2]:

$$\frac{g_m}{I_D} \approx \frac{1-e^{-\sqrt{IC}}}{nU_T\sqrt{IC}} \approx \frac{1}{nU_T\left(\sqrt{IC+0.25}+0.5\right)} \qquad (3)$$

Unchanged, W.I.

$\downarrow \propto \frac{1}{\sqrt{IC}}$, S.I.[2]

DC Mismatch and Flicker Noise

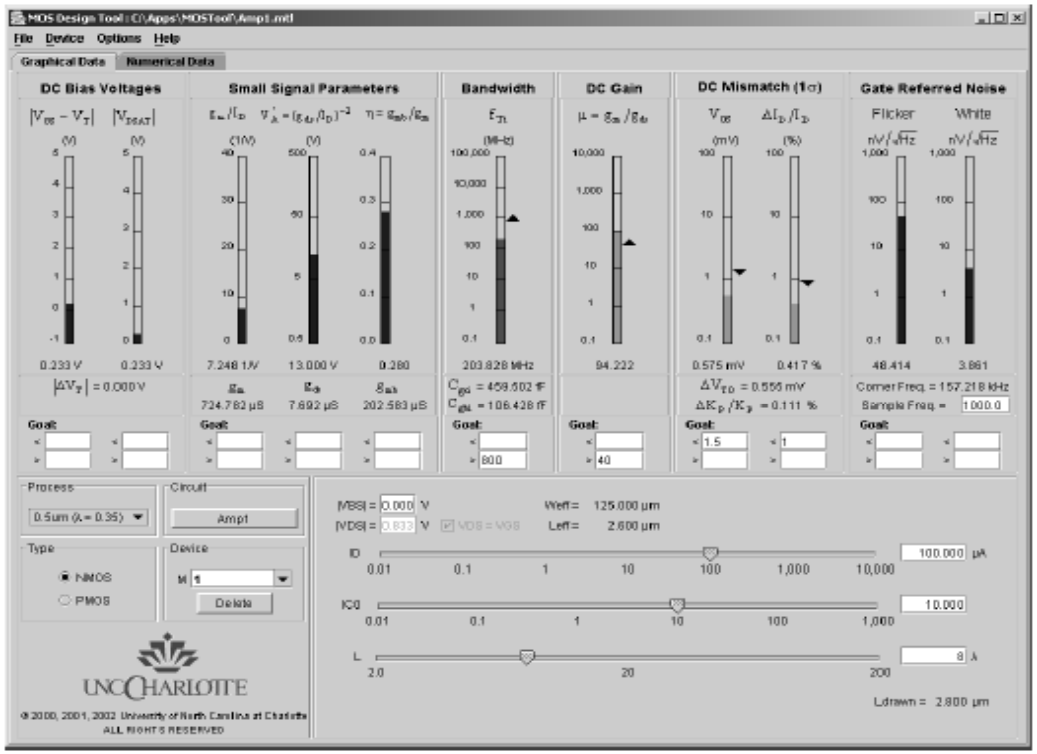
- I_D mismatch due to threshold voltage mismatch
- DC mismatch and input-referred flicker noise voltage are minimized by maximizing gate area.
- Operating in weak IC and long L is also where max MOS gain is obtained

TABLE IV
MOS DC MISMATCH AND GATE-REFERRED FLICKER NOISE RELATIONSHIPS

Parameter	$IC\uparrow$ L, I_D fixed	$L\uparrow$ IC, I_D fixed	$I_D\uparrow$ IC, L fixed
Threshold Voltage Mismatch: $\Delta VTO = \frac{AVTO}{\sqrt{WL}} = \frac{\sqrt{IC_0}}{L}\sqrt{\frac{I_0}{I_D}}AVTO$ (1)	$\uparrow \propto \sqrt{IC_0}$ $(WL \propto \frac{1}{IC_0})$	$\downarrow \propto \frac{1}{L}$ $(WL \propto L^2)$	$\downarrow \propto \frac{1}{\sqrt{I_D}}$ $(WL \propto I_D)$
Transconductance Factor Mismatch: (generally negligible for $IC < 100$) $\Delta KP = \frac{AKP}{\sqrt{WL}} = \frac{\sqrt{IC_0}}{L}\sqrt{\frac{I_0}{I_D}}AKP$ (2)			
Body-Effect Factor Mismatch: (present only for nonzero V_{BS}) $\Delta\gamma = \frac{AGAMMA}{\sqrt{WL}} = \frac{\sqrt{IC_0}}{L}\sqrt{\frac{I_0}{I_D}}AGAMMA$ (3)			
Gate-Referred Flicker Noise Voltage: $S_{V\,flicker}^{1/2}(f) = \sqrt{\frac{K_F}{C_{OX}^2 WLf^{AF}}} = \frac{1}{\sqrt{WL}}\sqrt{\frac{K_F}{C_{OX}^2 f^{AF}}} = \frac{\sqrt{IC_0}}{L}\sqrt{\frac{I_0}{I_D}} \bullet \sqrt{\frac{K_F}{C_{OX}^2 f^{AF}}}$ (4) $(\frac{V}{\sqrt{Hz}})$			

CAD Design Tool

- MOS circuit performance evaluated by
  a) Linkage to commercial SPICE-like simulator that can run EKV and BSIM3 models
  b) Linkage to custom MOS model equations which may modify existing MOS model
  c) Linkage to arrays of measured MOS data
- User interface allows designer to select design parameters as well as desired performance specs and dynamically display tradeoffs using colored bar graphs.



CAD Tool Example

ILLUSTRATION OF NMOS SIZING OPTIMIZATION

Design Inputs			**Resulting Circuit Performance**									
			Lay-out	Min. V_{DS}	Small signal Parameters			Band-width	DC mismatch (1σ)		Gate referred noise voltage	
I_D	IC_0	L	W	V_{DSAT}	g_m	g_{ds}	A_{Vi}	f_{Ti}	$\Delta I_D/I_D$	ΔV_{GS}	white	flick.[1]
µA		µm	µm	V	µS	µS	V/V	MHz	%	mV	nV/(Hz)$^{1/2}$	
100	10	0.5	24	0.25	657	40.0	16.4	4,997	1.98	3.02	4.06	251.8
100	10	1.2	58	0.24	705	16.7	42.3	931	0.88	1.25	3.92	104.9
100	10	2.6	126	0.23	725	7.69	94.2	204	0.42	0.58	3.86	48.4
100	1	1.2	578	0.14	1670	16.7	100	286	0.64	0.38	2.54	33.2
100	10	1.2	58	0.24	705	16.7	42.3	931	0.88	1.25	3.92	104.9
100	100	1.2	5.8	0.79	223	16.7	13.4	2,714	1.14	5.11	6.96	331.7

- NMOS xtr at ID = 100uA, 0.5um CMOS process
- Intrinsic voltage gain Avi > 40 V/V

  Intrinsic bandwidth fTi > 800MHz

  DC current mismatch < 1% (1 sigma) (current mirror)

  DC voltage mismatch < 1.5 mV(1 sigma) (diff. pair)
- Short L, BW met, Avi, mismatch not met.
- Long L, Avi, mismatch met, BW not met.

Conclusions

- Transistor level design methodology can produce optimal drain current and sizing for use in any analog circuit topology using ID, IC and L to find W
- Exploring the performance of a transistor operating at different inversion levels can benefit circuit performance and expand design options
- Every MOS xtr operates in the MOS operating plane from which tradeoffs between a variety of performance criteria can be explored
- CAD tools can be designed to implement advanced behavior of MOS transistors and optimize them based on the relationships established with inversion level as a design parameter
- Device optimizations can be done before circuit simulations to reduce trial and error simulations while considering high order effects

Reference:

A CAD Methodology for Optimizing Transistor Current and Sizing in Analog CMOS Design, D.M. Binkley, C.E. Hopper, S.D. Tucker, B.C. Moss, J.M. Rochelle, D.P. Foty

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol.22, No. 2, February 2003