A 100V High Voltage Phase-Programmable Electrode Driver Array in 1.0 micron CMOS SOI Technology for a Fluidics Processor Application

by

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Abstract

Using micro-scale fabrication and high voltage technologies, a fluid analysis system based on the transportation of fluid droplets by dielectrophoresis (DEP) can be developed. This thesis describes the development of a two-dimensional high voltage phase programmable driver array serving as the engine for a programmable fluidics processor (PFP) system employing DEP. The planar electrode array consists of 32-by-32 high voltage drivers, each capable of producing square waves of up to 100V which can be programmed between two phases: 0-degrees and 180-degrees in-phase with a square wave reference. By programming sequential phase changes of the array's square wave outputs, a droplet movement path can be configured for the transport of a fluid droplet sample and its movement response can be studied. High voltage is necessary to generate the force needed to transport drops between electrodes in a lateral direction. The chip is produced in high-voltage 1.0um SOI technology, which allows the integration of the 100V driver circuitry and 5V CMOS control circuitry on a single chip making it a candidate for a laboratory-on-a-chip application. The chip is designed as part of a prototype portable system and has shown to be capable of transporting drops across its coated surface. Circuitry allowing for DEP assisted injection of droplets onto the coated surface of the PFP chip is also presented.

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This work is dedicated to those people who have helped me throughout the years whom I hold dearest. To my ma, Tsu Ying Yuk, and my ba, Hung Nin Yuk, for giving me life and endlessly sacrificing themselves to ensure a future for me. And to my goh-goh, Michael Yuk, for all those years growing up together.

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Chapter 1 Introduction to a Programmable Fluidics Processor Integrated Circuit for the Programmable Fluidics Processor System

1.1. Introduction to the PFP IC

A programmable array of high voltage electrode drivers capable of producing 100V square-wave signals with two-state phase change capability for use in a prototype programmable fluidics processor (PFP) system is developed. The goal of the PFP system is to implement an environment for controlled fluid droplet movement utilizing an effect called dielectrophoresis (DEP). The PFP integrated circuit (PFP IC) serves as the engine for the PFP system in that it provides the high voltage signals and electric fields necessary to produce the required DEP forces for fluid droplet movement.

The specifications for the chip are provided by the members of the University of Texas MD Andersen Cancer Center (UTMDACC) who have conducted extensive research on DEP and its applications. The physical specifications require a driver array of 1024 cells arranged in 32 rows by 32 columns each having an electrode of 100um square with 100um vertical and horizontal spacing between electrodes. The electrodes need to be placed at the topmost metal layer to allow close interaction with the external world. For the electrical specifications, each driver cell must be capable of producing a 100Vpp AC square-wave whose phase can be individually programmed to either 0 degrees or 180 degrees in-phase with the input reference signal. Additionally, the column of electrodes at the far end of the chip must be capable of a third, ground output state for the purpose of droplet injection. An operating frequency of 10kHz for the electronics is desired. A peak

output voltage of 100V is necessary to produce the electric fields needed to induce enough DEP force to transport a droplet between electrodes. AC signal outputs are used to allow testing of a droplet's response to frequency and thus phase differences between electrodes are actually alternating potential differences that create the DEP forces. The capability of programming each phase output allows for precise control of the droplet movement path.

The PFP IC realizes high voltage output through the use of high voltage silicon-on-insulator (SOI) technology. SOI technology allows the integration of high voltage driver electronics with low voltage control circuitry on a single substrate due to its inherent isolation characteristics. The advantage of such integration onto a single chip results in a high voltage device that is both compact and efficient in terms of maximizing on-chip circuitry while minimizing off-chip interconnects. The logic circuitry in the PFP IC uses 5V CMOS technology, and the high voltage electrode driver uses resistor loaded high voltage NMOS pull-down transistors capable of 100V operation.

For the prototype PFP system, the PFP IC is used in conjunction with a Micro Electro Mechanical Systems (MEMS) fluidics chamber that lies atop the PFP IC, a fluidic valve system and control hardware and software. The PFP IC chips are designed by Wayne Current, Kelvin Yuk, Harriet Lam and Alec Wong of the University of California, Davis (UCD) and fabricated through X-Fab Semiconductor using the 1.0um SOI CMOS high voltage technology, XI10. The chips were tested jointly by UCD and Chuck McConaghy of Lawrence Livermore National Laboratory (LLNL). The MEMS chamber and fluidic

system is designed by Peter Krulevitch of LLNL, and the control hardware and software is designed by Craig Andrews of Lynntech, Inc College Station, TX.

1.2. PFP IC System Overview

1.2.1. PFP IC System Components

The PFP IC is composed of two major parts: the driver circuitry and the communications circuitry. The driver circuitry is essentially the 32-by-32 high voltage array, composed of digital driver cells, each containing enabling logic that allow for the cell's memory to be uniquely addressed, a 1-bit memory for storing the phase state of the output signal and a digital driver circuit which produces the 100V high voltage output and allows either an in-phase or out-of-phase output relative to the reference square-wave signal depending on the cell's stored phase data. The driver array also has additional circuitry that enables the column of electrodes at the far end of the chip to realize a third, ground state. The communications circuitry is composed of an 11-bit communications shift register, decoders for the 5-bit row and 5-bit column addresses and data buffers for the intermediate signal lines. The 11-bit communications shift register is serially loaded and stores the 1-bit input phase data to the target driver cell, and the 5-bit row and 5-bit column addresses of the target driver cell. The address decoders decode the address data from the shift register and activate the corresponding row and column lines on the array, which in turn enables the memory of the targeted driver cell.

1.2.2. PFP IC System Operation Summary

The PFP IC requires thirteen external lines for full functionality of the communication, driver and injection components. The signal names and their descriptions are summarized in Table 1-1. The details of the full-sized prototype chip are given in Chapter 4 and a summary of the chip operation is given here. Programming of the PFP IC encompasses addressing a driver cell and setting the phase state of its output. Upon reset, the data in all the cells are logic low and the electrode outputs are out-of-phase with the reference square-wave. During programming, a desired cell is selected by feeding the DATA_IN input with the 5-bit column address, 5-bit row address and 1-bit phase data of that cell. Once the address and data are present in the shift register, the LOAD signal controlling the output of the shift register is enabled high and the data are passed to different parts of the circuit. The 5-bit row address is passed to the row address decoder and the 5-bit column address is passed to the column decoder. The 1-bit data signal is sent to data inputs of all the digital driver cells.

Table 1-1 Input and control signals for the PFP1K prototype engine

Signal Name	Function
CLRB1	Resets the Shift Register memory
CLRB2	Resets the Driver Cell memories
DATA_IN	Serial input to the shift register for reading the new phase state and addresses
CLK	Shift register enable signal
LOAD	Controls the passing of the valid addresses from the shift register to the decoders and the new phase data from the shift register to the array driver cells.
EN1B	Enables the input latch of the master-slave dual latch of the targeted driver cell
EN2B	Enables the output latch of the master-slave dual latch of the targeted driver cell. Once activated following EN1B, the electrode outputs of all cells are updated with their new phase state memory.
VIN	Serves as a reference signal for the digital driver outputs. The phase of the digital driver outputs will be either 0-degrees or 180-degrees in-phase with VIN depending on the cell's stored data
INJ	Input data to the ground state injection column circuitry
REFINJ	Voltage at the injection reference electrode
V5	Supply voltage for the CMOS logic
V100	Supply voltage for the high voltage output driver
VSS	Ground reference voltage

The decoders then activate the row and column lines corresponding to the addresses. Once the correct row and column lines are enabled, EN1B is pulsed from high to low and the cell at that array location stores the new data into its memory. At this point, the output of the cell has not yet been updated, only the new data has been stored. This programming cycle can be repeated for as many of the cells as desired. Once programming is complete, all array outputs are simultaneously updated with the new data by pulsing EN2B from high to low. The process of simultaneously updating the electrode outputs prevents premature changes in the outputs of individual cells as they are programmed sequentially.

1.3. Development Stages of the PFP IC

The evolution of the PFP IC into a fully characterized and operational system takes place over several development stages. The results provided in this work is a culmination of the data acquired from three test chips.

1.3.1. Programmable Fluidics Processor version 2 (PFP2)

The PFP2 test chip is the first SOI test chip made during the development of the PFP IC. It was designed by Alec Wong and tested by Kelvin Yuk and Harriet Lam. The purpose of the chip is to test the communications circuitry on a smaller sized high voltage driver array. The PFP2 test chip contains two 4-by-4 driver arrays that share address and phase data from a common communications shift register. Each array has its own 2-bit row decoder but share a 2-bit column decoder. The driver arrays use analog high voltage drivers rather than digital drivers to produce sine wave outputs instead of square wave outputs. A sine wave output is ideal in that it contains no harmonic components found in digital signals. To investigate possible options for the loading of the high voltage driver, one of the high voltage arrays uses active loads while the other uses resistive loads. The PFP2 chip also contains various analog driver test cells using active and passive loads.

Unfortunately, numerous critical layout errors were found while testing PFP2. The lack of a design rule checker for this technology and schematic extraction capabilities also made error checking difficult. In one error, the source and drain of the transistors in the decoders are reversed and prevent proper activation of the row and columns lines. In another layout error, two transistors of the analog driver cell have their sources and drains

reversed. The SOI process used does not allow the reversal of the source and drain in a transistor, resulting in incorrect operation of the analog drivers.

1.3.2. Programmable Fluidics Processor version 3 revision 11/19/02 (PFP31119)

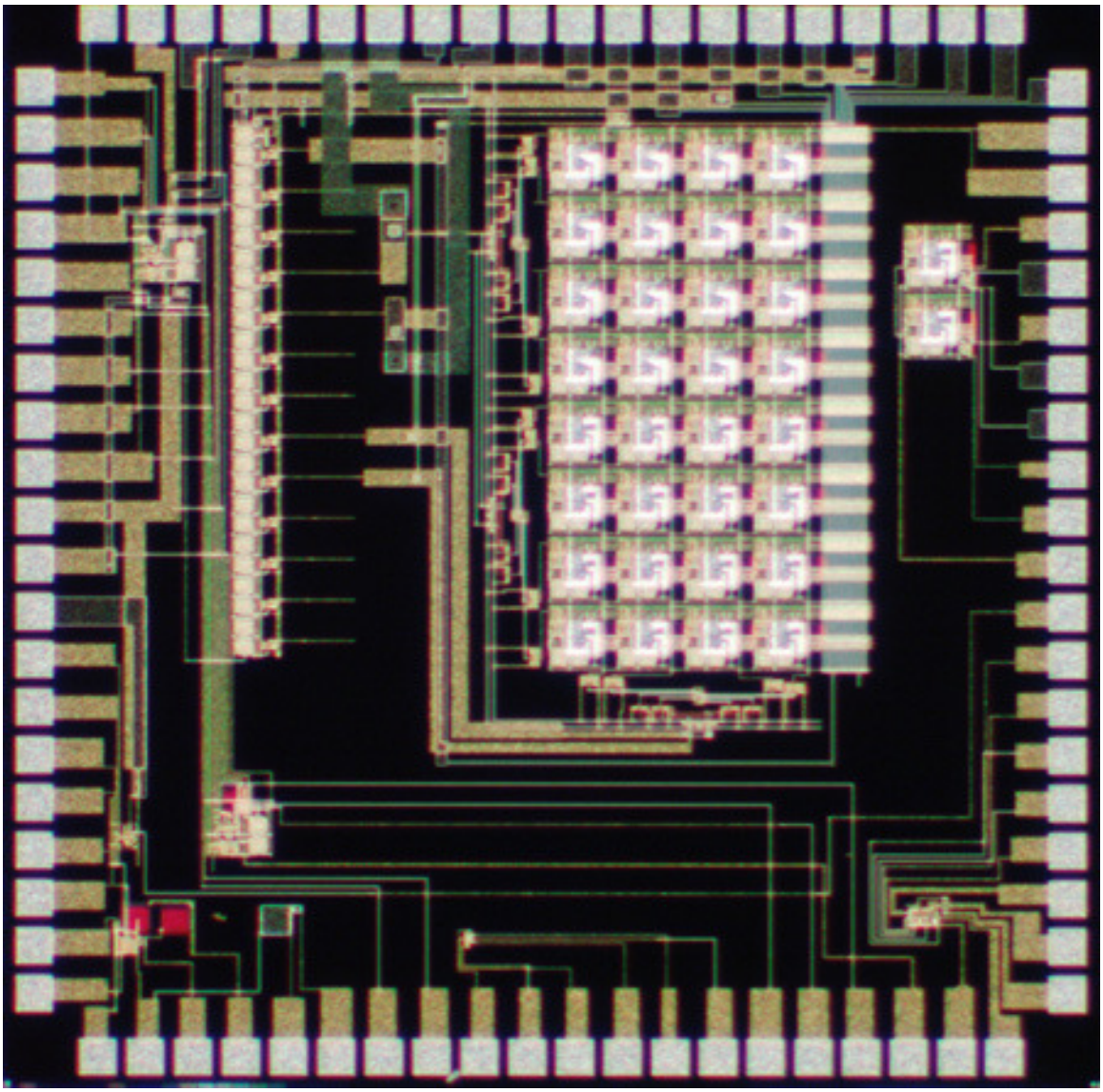

Figure 1-1 PFP3 rev. 11/19 chip (PFP31119) photograph

The PFP31119 chip is the second SOI test chip designed by Harriet Lam and Kelvin Yuk and is shown in Figure 1-1. The goal of PFP31119 is to correct for the errors made in PFP2 and to test a scaled-down version of the PFP electronics. Like PFP2, the PFP31119

chip contains two 4-by-4 high voltage driver arrays that each has its own 2-bit row decoder but share a single communications shift register and 2-bit column decoder. Unlike PFP2, one of the arrays in PFP31119 uses resistor loaded analog drivers while the other uses resistor loaded digital drivers. The use of digital drivers arises from the difficulty in testing and biasing the analog driver circuits and thus is used in favor of the analog driver. According to [1], square waves have been successfully used in many DEP droplet movement experiments. Additionally, digital drivers simplify the signaling requirements of the driver cell and replace the analog drivers on the full-sized prototype chip, PFP1K.

The PFP31119 chip has holes in the passivation layer to allow for probe testing of the electrode outputs. The PFP31119 has test circuits consisting mainly of the high voltage analog driver in different loading and device width configurations. The chip also has a high voltage digital electrode driver test circuit.

1.3.3. Programmable Fluidics Processor version 1K (PFP1K)

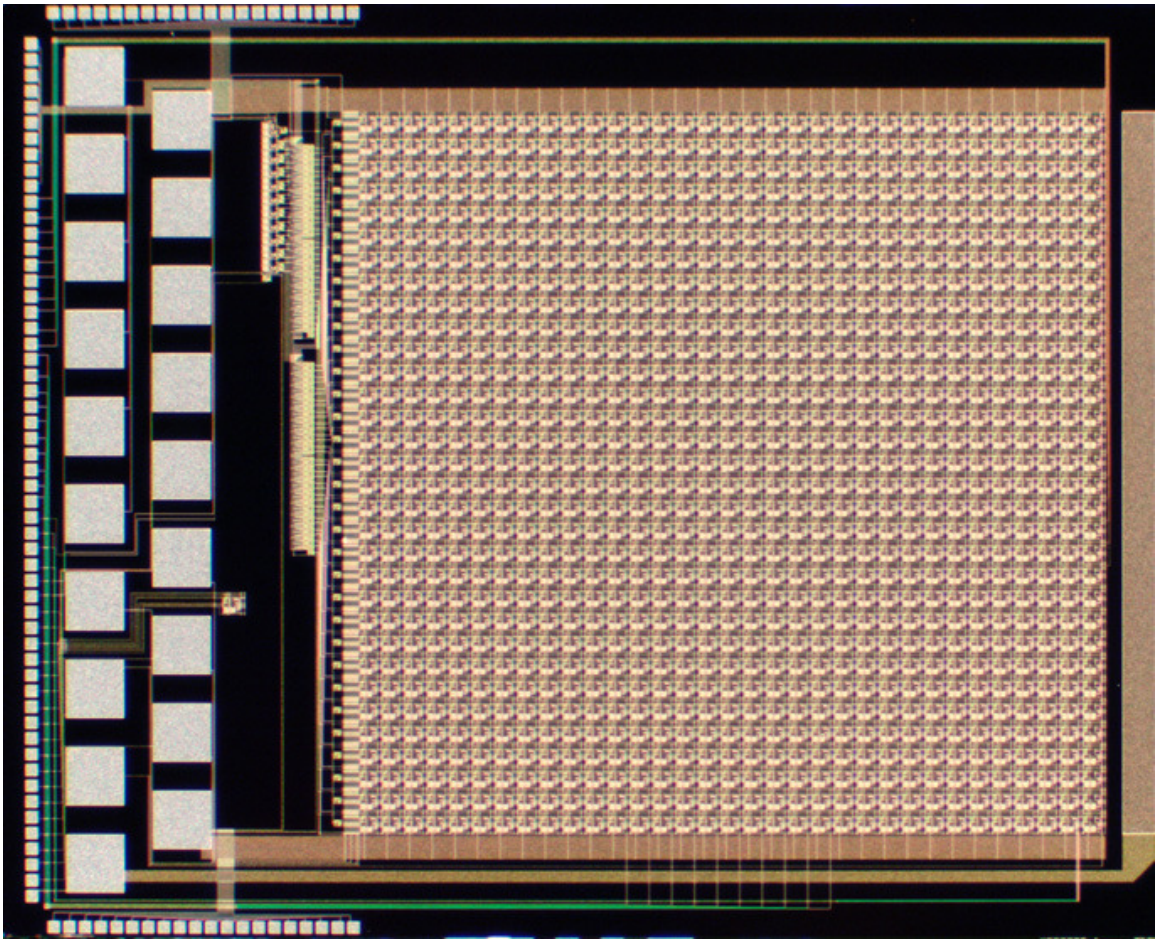

Figure 1-2 PFP1K chip photograph

The PFP1K chip is the third SOI test chip and a full-sized prototype of the PFP electronics. It is designed and tested by Harriet Lam and Kelvin Yuk and is shown in Figure 1-2. It is composed of a 32-by-32 element driver cell array, an 11-bit communications shift register, a 5-bit row address decoder, a 5-bit column address decoder, data buffers, a reference injector electrode and injector electronics. The injection electronics are integrated into the array as an additional column of cells that when used in conjunction with the reference injector electrode can assist droplet injection into the MEMS structure. The PFP1K chip's vital control signals are wired to large pads,

which are due to be vertically routed by micro spring loaded pins and to bond pads, along with many other intermediate signals, allowing for complete testing of the individual system components.

The PFP1K also has a digital driver test cell complete with enable logic, a 1-bit master-slave memory element and an output driver with electrode. The digital driver test cell (DDTEST) allows for direct testing of an array cell that was not available on PFP2 or PFP31119. Unlike PFP31119, the passivation layer does not have holes above the array electrodes in PFP1K, preventing direct probing of the electrodes. An unbroken passivation oxide is required in the prototype to allow mounting of the MEMS fluid device on top of the chip's surface. For testing purposes, the oxide can be scratched off using a microprobe to access the electrodes and has been successfully done so in many tests.

1.4. Accomplishments of the PFP IC

Through extensive simulation and testing of both PFP31119 and PFP1K chips, the PFP1K chip is a success in that the communications and programming circuitry is operational and that the digital driver can produce 100V square wave signals and change the phase of the signals based on the output cell's stored data bit. The functionality of the communications circuitry was verified by individually testing the communications shift register and decoders through intermediate signal lines. The digital driver test cell was programmed with phase changes to test the addressable memory logic and driver output capability. Once all individual parts of the PFP IC were tested, the functionality of the

entire chip was verified by performing programming cycles of phase changes on various array driver cells. A programming cycle simulates realistic control of the system through the input signal lines. Changes in the phase of the output signals at the desired locations were observed, confirming correct operation of the driver logic, driver memory as well as the communications shift register, decoders and signal buffers. Testing of PFP1K is described in detail in Chapter 5.

Further testing by UTMDACC proves that the PFP IC is able to produce the necessary forces needed for droplet transport and is capable of transporting droplets across a coated array surface although under strict operating conditions. These experiments and results are discussed in more detail in Chapter 5.

Some of the performance requirements for the PFP IC, however, either cannot be verified or were not met. These include the clock frequency goal and the correct operation of the injector electronics. The output frequency of the electrodes is limited to about 100Hz probably due to the large load resulting from the electrode and the probing method used. The injection circuitry does not operate correctly and the injection column's electrode outputs are not capable of realizing three distinct output states. This is due to a layout error shorting all the electrode outputs in the injection driver column. The corrected version will be available in the next version of the chip, PFP5. The chip performance and errors are discussed in Chapter 5.

1.5. Scope of the Thesis

Chapter 1: Introduction to Programmable Fluidics Processor Integrated Circuit for the Programmable Fluidics Processor System

In Chapter 1, the PFP IC developed as the engine for the PFP project is presented. An overview of the system components, functionality and control signals is given, followed by a briefing on the development stages of the electronic chips and a summary of the accomplishments of the PFP IC.

Chapter 2: PFP System Background

In Chapter 2, the concept behind PFP is discussed. Chapter 2 covers the basics of DEP forces as well as an overview on the entire PFP project including droplet manipulation by DEP, the prototype bench top test version of the PFP system constituting the PFP IC, the MEMS fluidic chamber, DEP assisted droplet injection and the interface system used to set the droplet movement path.

Chapter 3: High Voltage Technology used in the PFP chip

Chapter 3 discusses high voltage technology and high voltage transistor design. Understanding the capabilities of high voltage technology allows proper design of the circuitry needed for the PFP IC to implement DEP. Design of a widely used high voltage transistor, the laterally diffused MOS (LDMOS), is presented and the design parameters affecting the breakdown voltage of these devices are discussed. The high voltage transistor characteristics of the X-FAB XI10 technology will be discussed briefly and a comparison between the simulated and experimental performance of the transistors used on the PFP IC is given.

Chapter 4: PFP chip electronics details

In Chapter 4, the circuitry of the individual components of the PFP electronics will be covered in detail. First the memory elements used in the PFP IC will be discussed. Then, the array driver cell will be described by its high voltage output driver, memory latch and enable logic. The arrangement of the digital driver cells into the array and the routing of its signals will be described. Next, the communications circuitry composed of the shift register and address decoders will be discussed. The design and HSPICE optimization of the data buffers for the intermediate signals with large fan-out will be given. Finally, the droplet injection three-state electronics will be described.

Chapter 5: PFP chip results

In Chapter 5, the testing of the PFP1K chip by both UC Davis and UTMDACC is described. The electrical tests conducted by UCD are presented first. The test setup and overall procedure is given. Then, the experiments and results conducted on the PFP1K chip are presented first with the tests that verify the operation of the programming circuitry and the high voltage output of the driver cell and then with the injection circuitry. A discussion and further test results explaining the effects of probe loading and the early update of the output phase and the injection circuitry layout error are given. Following that, the droplet transport experiments conducted by UTMDACC will be described along with the conditions and procedure for which droplet movement was successfully performed.

Chapter 6: Summary and Conclusions

Chapter 6 contains a summary of the work presented here, highlighting on the key points of each chapter. The important results of the chip testing are reiterated. Some points on improvements to the PFP1K chip and further research are discussed.

References

[1] J. Schwartz, UTMDACC, (email communication), January 7, 2004

Chapter 2 Programmable Fluidics Processor System Background

Chapter 2 will discuss the motivation of PFP, explain dielectrophoresis as the mechanism for fluid transport within PFP, give an overview of the PFP architecture and the prototype system, and describe DEP assisted droplet injection and the PFP system interface.

2.1. Motivation of a Programmable Fluidics Processor (PFP)

2.1.1. Introduction

Realization of a laboratory on a chip for chemical and fluid analysis has been researched for many years. Miniaturizing the scale at which fluid analysis can be performed has many clear advantages in chemical and biological applications. A micro-scale device is portable, robust and durable, less prone to contamination due to a highly accurate metering of reagents and reduced environmental exposure, and efficient with sample usage through scaling of the analysis environment. System portability is significant in that the analysis system can be brought to a sample in the field and processed there rather than the sample being brought back to a lab. Directly sourcing the fluid under study allows a larger supply of the sample and reduces overhead. By keeping the reagents in a pressured microsystem, the chances of exposure to air-born and other environmental contaminants may be reduced and may result in better yield. By using smaller sample amounts per analysis, analyses can be repeated, reducing material costs and space usage. Scaling of the system in this manner saves time and allows processing in a parallel fashion.

2.1.2. PFP System Goals

The goal of PFP is to meet the challenges of a portable laboratory on a chip by realizing a general-purpose diagnostic device to discriminate and manipulate matter through dielectrophoretic control [1,2,3]. Dielectrophoresis is the movement of polarizable fluids in a non-polarizable medium by subjecting them to inhomogeneous electric fields. The expectation is that by realizing an integrated, programmable environment for dielectrophoresis, fluid can transported by programming a desired droplet movement path and analyzed based on its behavior to different excitation frequencies. The advantage of programmability is ease of use and process automation, both of which can reduce human error and lead to better results.

The vision for the complete PFP system is a fully integrated wristwatch sized device. The PFP IC designed for this application of a PFP system are to be used for a prototype benchtop test device described in more detail in Chapter 2.3.6.

2.1.3. Applications of PFP

There are many potential applications for PFP in the areas of public health, medicine, chemical and biological fluid analysis and military. For example, in analyzing water composition, PFP can be used for purity testing and pollutant or poison identification. Dielectrophoresis has shown effect on biological cells, implicating many possible applications in medicine and cancer research. The distinct dielectric properties of different cell types can be exploited to characterize, manipulate, fractionate, isolate, trap

and burst them [3,4]. As a portable lab device, chemical manipulations by sorting, isolating, trapping and combining can also be performed [3,4]. Another application is in chemical and biological warfare detection for the military. For example, soldiers on the battlefield in the presence of chemical agents can test their exposure using wristwatch-sized PFP units. In general, some of the goals of PFP are to be able to move, combine and separate droplets using DEP forces.

The challenges in designing the programmable fluidics processor involve fabricating a micro-scale reaction chamber to facilitate fluid manipulation, implementing a scheme for injecting the fluid droplets into this chamber, designing the electronics capable of realizing high voltage signals and controlling the electronics in a programmable fashion through an external interface. This thesis focuses on the design of the electronics needed to control and produce the high voltage signals for DEP manipulation.

2.2. Principles of Dielectrophoresis (DEP)

In order to realize fluid analysis in a compact, portable device, a method of characterizing fluid droplets is needed. One method is through dielectrophoresis (DEP) and is the basis for which PFP operates. In dielectrophoresis, the movement of fluids in a channel-less chamber by electrical field forces can be exploited to discriminate and characterize fluid samples by their dielectric properties [1,2,3]. This discussion is an adaptation of [1] and explains the principle concepts of dielectrophoresis and how it can be utilized to induce the movements of different droplet types.

In an application of dielectrophoresis, a fluid droplet is placed within some fluid medium and an electric field is applied on the droplet. There are two requirements for droplet movement to occur: (1) either the fluid droplet is more polarizable than the medium, or the medium is more polarizable than the droplet and (2) the applied electric field is inhomogeneous. The following first discusses the case where the droplet is polarizable and the medium is non-polarizable and then the case where the droplet is non-polarizable and the medium is polarizable.

DEP force in action is illustrated in Figure 2-1 on a polarizable particle within a non-polarizable medium. A positive voltage is applied on the spherical electrode to the right of the particle, while a negative voltage is applied on the electrode plate to the left of the particle creating an inhomogeneous electric field between the electrodes due to their different sizes and shapes. This inhomogeneous electric field will polarize the particle: negative charges within the particle will migrate toward the right while positive charges will migrate toward the left. Since the field is inhomogeneous, the field gradient is stronger on the end of the spherical electrode and causes the particle to move to the right. This type of dielectrophoresis where the particle is attracted to the high field region is called positive DEP.

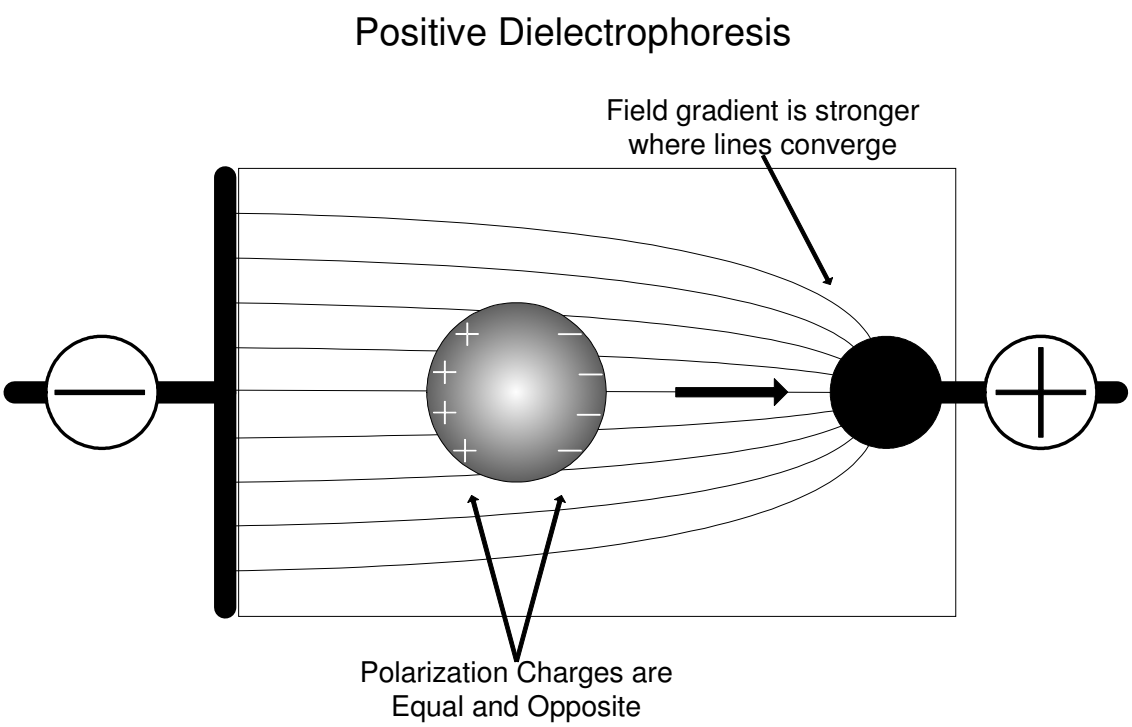

Figure 2-1 Positive Dielectrophoresis [1]

In the complementary case, an electric field is applied to a non-polarizable particle in a polarizable medium as shown in Figure 2-2. Here, instead of the particle polarizing with positive charges migrating to the low field region and negative charges migrating to the high field region, the medium itself polarizes and as a result, negative charges in the medium migrate to the high field region and positive charges the medium migrate to the low field region. As a result, the particle experiences a DEP force repelling from the high field region. This type of dielectrophoresis is called negative DEP.

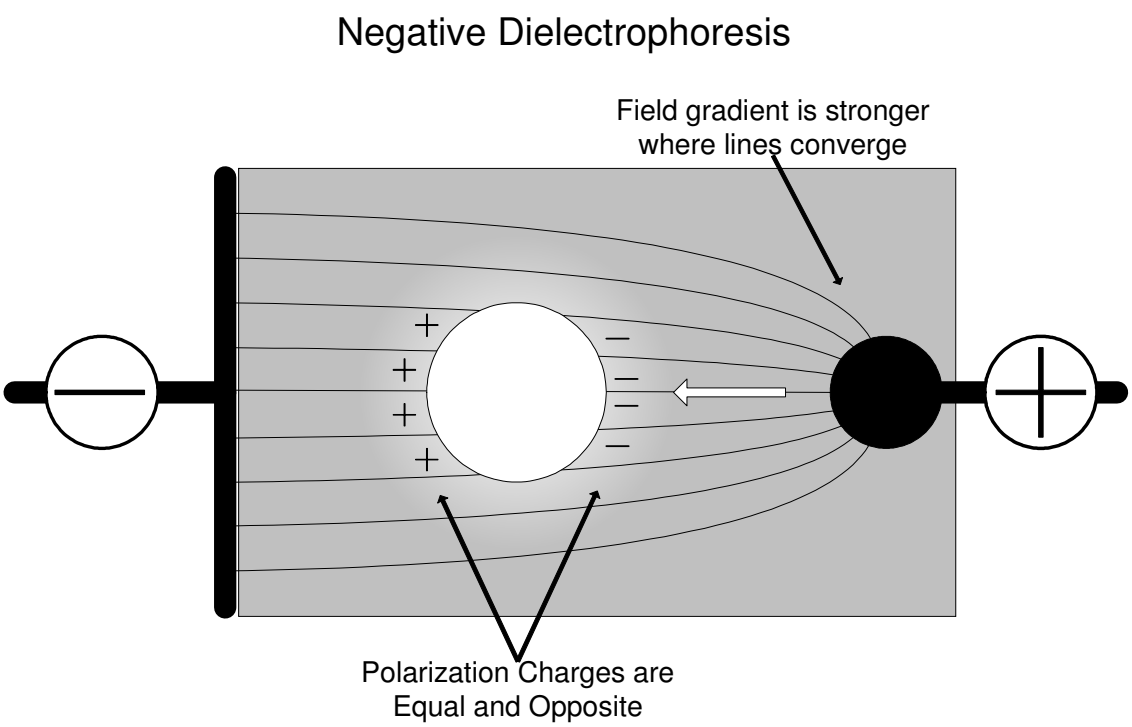

Figure 2-2 Negative Dielectrophoresis [1]

The examples illustrate positive and negative DEP forces generated by DC electric fields. If in positive DEP, an AC electric field were used, the polarization of the particle will alternate as the polarity of the field alternates resulting in particle movement in the same direction as in the DC case. The changing of polarization of the particle takes time and the particle's response to the alternating electric field is dependent on its unique dielectric properties. At very low frequencies, the charges in the particle may have sufficient time to change polarizations and the DEP force and droplet movement may resemble the DC case. However, at higher frequencies, the particle may not be able to change polarizations quickly enough to compensate for the alternating electric field. The result is a weaker DEP force and weaker droplet movement.

This phenomenon can be exploited in that the DEP forces and movement of an unknown particle under an applied AC voltage can be used to infer the particle's dielectric properties. One of the application goals of PFP is to be able to apply AC signals at different frequencies onto fluid samples under experimentation.

From this discussion on dielectrophoresis, it is easy to see how the droplet movement by DEP forces can be exploited in useful ways. More information on dielectrophoresis, its effects and its applications can be found in [1].

2.3. Overview of the Development of a Microscale Droplet Manipulation System Using DEP

2.3.1. PFP System Capabilities

The PFP system is a microfluidics system built using Micro Electro Mechanical Systems (MEMS) and integrated circuit (IC) technology employing dielectrophoresis. The DEP forces are generated by high voltage electrodes and manipulation can be performed without physical contact. The advantage of using the proposed DEP-based programmable system is that it is channel-less, meaning no pumps and valves as found in traditional analysis systems [5]. As an electronically controlled system, it has on-the-fly programmability and reconfigurability making it versatile. The electrodes are arranged in a two-dimensional array, which allows for scalable control for variable droplet size manipulation.

2.3.2. PFP System Architecture

A conceptual illustration showing the architecture of the PFP structure is shown in Figure 2-3 [6]. The PFP system is composed of a MEMS fabricated fluidic chamber, the PFP IC, an interface board for producing the PFP IC control signals and interface with a personal digital assistant (PDA), and desktop PC software used to program the PDA with the desired droplet movement path. The MEMS fluidic chamber is a thin, channel-less, reaction area allowing two-dimensional movement of fluid droplets and is mounted on top of the PFP IC. It is filled with an inert, insulating fluid such as bromododecane, acting as the medium for droplet manipulation [6]. The bottom of the MEMS chamber surface is coated with a thin layer of hydrophobic coating that serves as the droplet movement surface. The thickness of the coating is optimized to allow for maximum DEP force on the droplets from the electrodes and is micro-roughened to prevent droplets from sticking to the surface [7]. At the sidewall of the MEMS fluidic chamber are microchannel ports from which fluid from reservoirs located elsewhere is injected into the chamber. The injection process is controlled by DEP using special electronics on the underlying chip as discussed in Chapter 2.3.5.

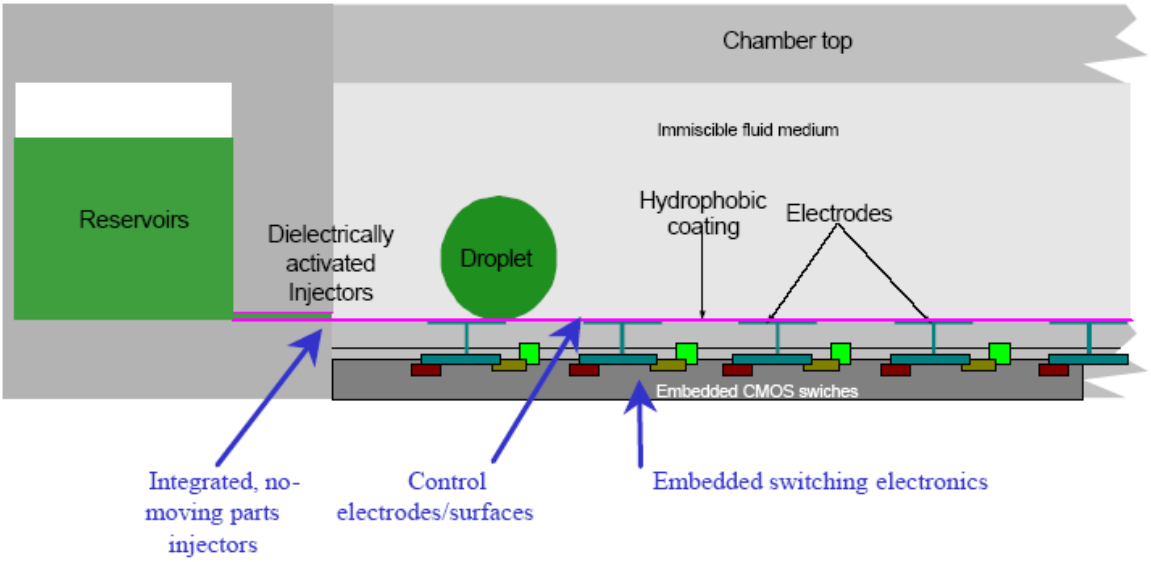

Figure 2-3 Proposed prototype PFP architecture [6]

2.3.3. DEP Forces of Various Electrode Shapes

The UTMDACC performed experiments to determine the optimal size and shape of the electrode, the spacing between electrodes and the thickness and type of passivation layer that coats the top of the electrodes. In their study, high voltage electrodes of different shapes were mounted on glass slides and characterized in terms of their DEP capabilities. The test description and data presented here are taken from [8].

Electrodes of four different shapes, squares, asterisks, stars and crosses, mounted on glass were tested for maximum DEP force capabilities shown in Figure 2-4. In the tests, two electrodes of each type are placed at a distance *s* from each other. The thickness of the Teflon passivation coating is varied and the DEP force between electrodes is measured [8]. The experiments were performed for several electrode spacings. In general, the maximum DEP force from the electrodes increases as the spacing between electrodes decreases. The optimal Teflon thickness at which maximum DEP force is achieved is

between 4um and 10um. The data shows that the square electrodes have the best overall performance.

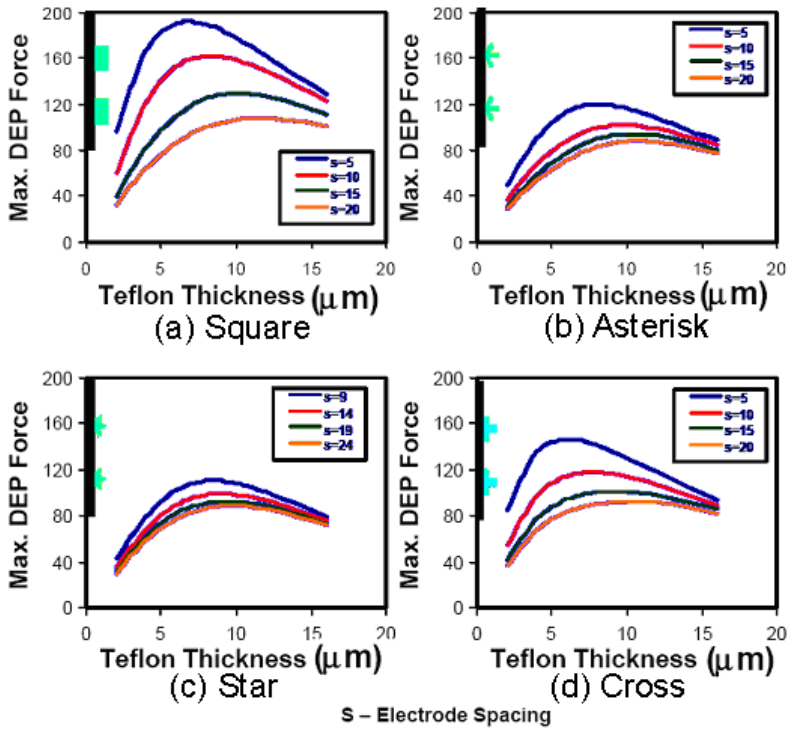

Figure 2-4 DEP force of electrodes on glass in difference configurations [8]

2.3.4. Droplet Control and Transport Across the PFP Surface by DEP

From the explanation on dielectrophoresis in Chapter 2.2, the requirement for positive DEP movement is that a polarizable fluid is surrounded in a non-polarizable medium in the presence of an inhomogeneous electric field. In the example used in the DEP explanation, the polarizable fluid droplet is placed in a non-polarizable medium and situated between two electrodes. One electrode is larger than the other such that a higher electric field gradient is present at the smaller electrode, causing the droplet to move toward that end. For the following explanation of DEP force on the electrode array, the

larger electrode will be referred to as the large DEP electrode while the smaller will be referred to as the small DEP electrode.

Although the electrodes on the PFP IC are on the same spatial plane rather than facing each other, the DEP forces are still generated. However, since all electrodes are uniform in size and shape, the large and small DEP electrodes for droplet movement are actually composed of a collective of the array electrodes in PFP. Since each electrode produces an AC square wave output whose phase is programmable to either 0 or 180 degrees in-phase with a reference square-wave input, programming the output of an electrode to a particular phase defines its role as either the part of the large or small DEP electrode.

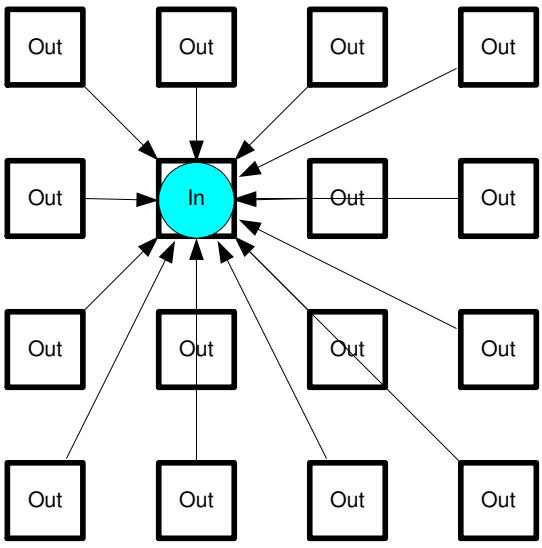

Figure 2-5 DEP force on a single electrode-sized fluid droplet

To illustrate, consider a small droplet situated atop an electrode within a 4-by-4 electrode array as shown in Figure 2-5. The electrode that the droplet rests on is 0 degrees in-phase (In) while all the other electrodes are 180 degrees in phase or out-of-phase (Out). The actual phases of the electrodes do not matter and are specified here only for illustration.

It is the voltage difference created by the phase difference between the electrode that the droplet rests on and all the other electrodes that matters. The electrode that the droplet rests on serves as the small DEP electrode with high electric field gradient since it has a phase output that is different from the rest of the array electrodes. All the other array electrodes collectively form the large DEP electrode with lower electric field gradient. Thus, the direction of the positive DEP force is toward the single in-phase electrode. As a result, the droplet is help in place above this electrode.

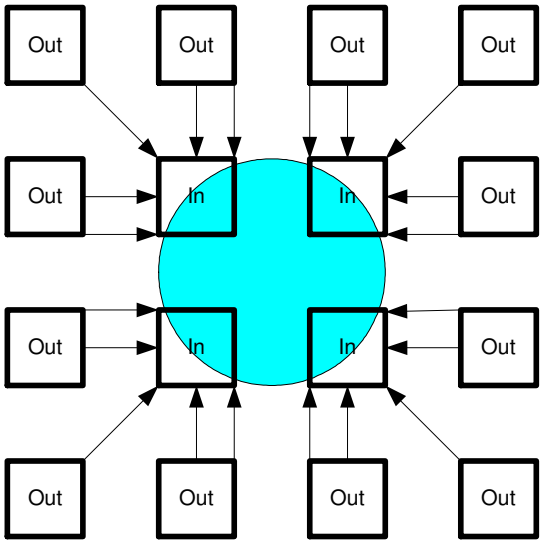

Figure 2-6 DEP force on a 2-by-2 electrode-sized fluid droplet

Now consider a larger droplet atop a 2-by-2 subarray of electrodes within the same 4-by-4 array of electrodes as shown in Figure 2-6. Here, the four electrodes that the droplet rests atop are in-phase (In) while all the outer electrodes are out-of-phase (Out). The electric field gradient is highest above the four in-phase electrodes since collectively they form the smaller DEP electrode while the outer electrodes collectively form the larger DEP electrode. As a result, a DEP force pulls the droplet toward the in-phase electrodes, keeping it in place.

In both cases, to move a droplet from one electrode location to the next, the small DEP electrode on which the droplet rests is programmed with a new phase data matching the large DEP electrode's phase, and the destination DEP electrode usually next to the starting location is programmed with a new phase data different from the large DEP electrode's phase. When the array outputs are updated, the DEP force originally holding the droplet in place will now change to the destination electrode with the different phase. The resulting force pulls the droplet array from its original location and toward its destination.

In the examples, the large DEP electrode is defined by the electrodes of the dominant phase, while the small DEP electrode is defined by the electrodes of the minority phase. It is more likely that if the electrodes composing the smaller DEP electrode are collectively localized, a higher DEP force can be realized. Also, AC signals are used in the examples by convention and because of its potential to characterize the behavior of the droplet based on its movement, which will be implemented on the actual PFP IC electronics. For these examples, DC voltages may also work and the polarity does not matter so long as a voltage difference exists between the small DEP electrode and the large DEP electrode.

2.3.5. DEP Assisted Droplet Injection

2.3.5.1.Motivation

The proposed scheme for injecting fluid droplets into the MEMS fluidic chamber uses DEP forces generated by certain array outputs. Using DEP to assist in injection makes the injection process controllable by the PFP hardware and integrates the injection scheme into the rest of the droplet manipulation system. First, the requirements for injection of fluid from an injector nozzle will be described. Next, the DEP assisted injection as performed in experiments by the UTMDACC will be described. Finally, the proposed injection scheme and hardware for the PFP IC will be presented.

2.3.5.2.Injection process and requirements

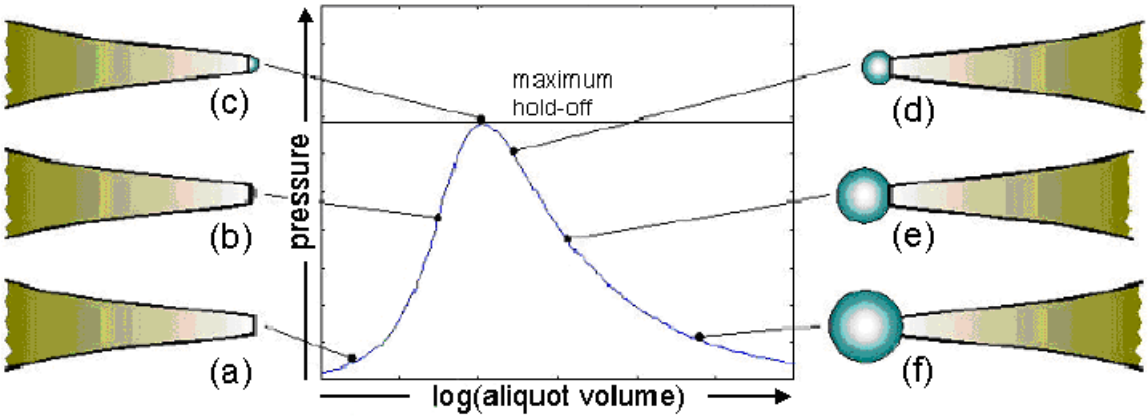

Figure 2-7 DEP Assisted droplet injection, modified from [6]

The fluid at an injector tip is characterized by its internal pressure, its volume beyond the injector orifice and the radius of the imaginary circle corresponding to the curvature edge of the fluid surface protruding from the injector orifice [5]. A plot characterizing the injection process in terms of internal pressure versus the volume of fluid beyond the injector tip is shown in Figure 2-7 [6]. In order for injection of fluid to occur, the internal pressure of the fluid within the injector tip must overcome the maximum hold-off

pressure identified in Figure 2-7. Initially, when the fluid at the injector tip is at low pressure (Figure 2-7a), the shape of fluid at the tip is fairly flat and has a low volume as shown in more detail in Figure 2-8a. Here, the internal hydrostatic pressure and the external laplace pressure are in equilibrium, holding the fluid within the injector orifice. As the internal pressure increases (Figure 2-7b), the fluid protrudes further out from the injector tip, increasing in volume and decreasing in radius. When the internal pressure is equal to the maximum hold-off pressure (Figure 2-7c), the radius of the droplet reaches a minimum equal to the radius of the injector orifice and the droplet forms a hemisphere extending from the orifice as shown in detail in Figure 2-8b. If the internal pressure is increased further, it will overcome the maximum hold-off pressure (Figure 2-7d), and the fluid will push out of the injector tip to relieve that pressure. The resulting droplet that forms on the surface has an increased radius and volume but with a lower internal pressure (Figure 2-7e,f).

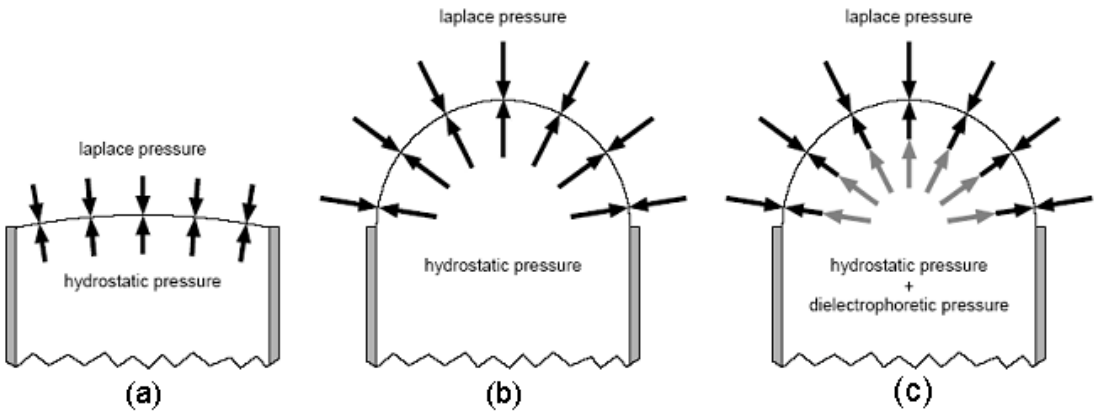

Figure 2-8 DEP Assisted Droplet Injection [5]

2.3.5.3.DEP Assisted Injection Performed by UTMDACC

In DEP assisted droplet injection, the internal pressure of the fluid at the injector tip is created by the hydrostatic pressure from the fluid reservoir plus a supplemental pressure generated by a DEP force between the injector tip and a droplet collection electrode as shown in Figure 2-8c. The hydrostatic pressure created by the fluid reservoir pressure is brought to a level just below the hold-off pressure so that when the collection electrode is activated and an electric field is created between the electrode and the injector tip, a supplemental DEP pressure will add to the hydrostatic pressure allowing the internal pressure to overcome hold off and cause injection of the droplet. The fluid droplets spontaneously form and collect at the collection electrode where droplets of arbitrary size can be made using metered units [5].

The UTMDACC conducted DEP assisted droplet injection experiments using micropipette fluid injectors and an electrode array on a glass slide. Initially, injection was successfully performed with a pipette whose voltage was left to float. Later, a ground strap was added to the pipette but had no perceivable effect on the injection [9]. High voltage AC square waves were used as the output signal of the collection electrode with voltages ranging from 120V to 270V depending on various electrical and mechanical parameters [9,10]. Droplet injection requires more voltage than droplet movement because the distance between the injector tip and the collecting electrode is greater then the distance between electrodes and because the DEP injection force needs to work against hydrostatic forces holding the fluid [9].

2.3.5.4.Proposed DEP Assisted Injection Scheme for the PFP IC

On PFP1K, the injectors are to be mounted on the right side of the chip and pointing left towards the last column of the electrode array. In the proposed injection scheme, the DEP force creating the supplemental pressure is generated by a potential difference between an electrode in the last column of the array serving as the collecting electrode and a reference electrode under the mounting location of the injector nozzle. Following the design requirements given by UTMDACC, each electrode in the column array has additional electronics that allow for a realization of a third output state of zero volts. In turn, it is possible for any of the electrodes in the last column to serve as the collection electrode during injection. Additionally, a large reference electrode is placed in the area beneath the location where the injectors are to be mounted in PFP1K as shown in Figure 1-2. The reference electrode is wired directly to a bond pad and can assume any arbitrary AC or DC signal. The reference electrode is added to PFP1K because the injector is mounted close to chip surface as opposed to in the pipette experiments and it may be important to directly control the voltage close to the injector tip [9]. The effects of using a reference electrode under the injector tip and its appropriate output signal are unknown and require further study.

With the addition of the three-state electronics and the reference electrode, various combinations of AC or DC potential difference can be created between the injector tips and the collection electrodes. This will allow more flexible study of the proposed injection scheme. The injection electronics are described in more detail in Chapter 4.7.

2.3.6. Prototype Benchtop PFP Test Device

2.3.6.1.Prototype MEMS Fluidic Chamber Cartridge

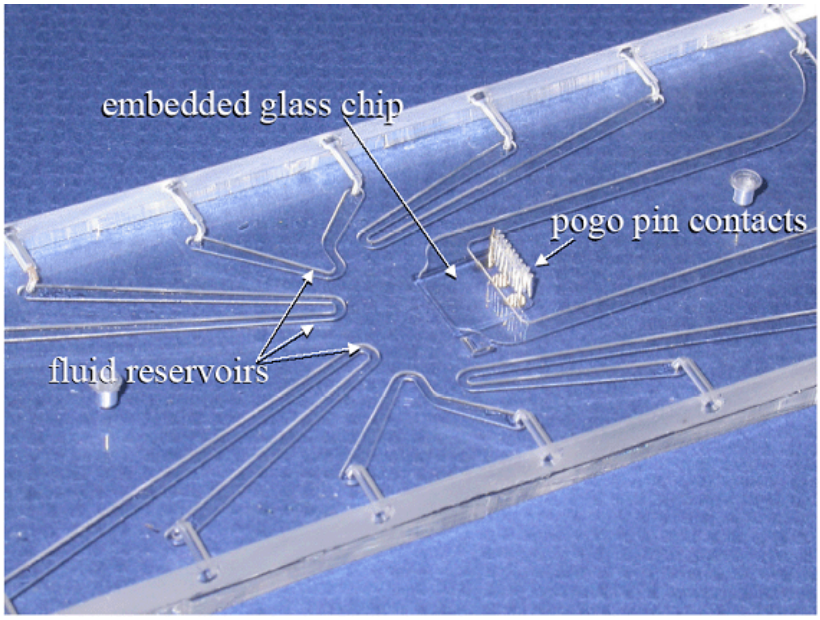

Figure 2-9 Photo of the MEMS cartridge showing the fluid reservoirs, embedded chip location and pogo pin contacts [11]

The MEMS fluidic device for the prototype PFP is designed by LLNL and is composed of a clear material called polydimethylsiloxane (PDMS). The chamber area, fluid reservoirs, and an embedded glass chip with electrodes are shown in Figure 2-9 [11]. Fluid is fed from an external source into the inlet port of a fluid reservoir and cycled through to its outlet port. The chamber itself has an inlet and outlet port for feeding in fresh fluid medium and flushing spent fluid medium. Each fluid reservoir has an injector channel at its bend that leads from the reservoir tip to the injection side of the MEMS fluidic chamber where the injection electrodes lie. This location is equivalent to the highest numbered column of electrodes. The injectors can be seen more clearly in the close up photograph in Figure 2-10 [11]. In both Figure 2-9 and 2-10, a square glass chip with electrodes is embedded where the actual electronics chip is to be placed. The

electronics chip is connected to external control hardware through vertical connector pins called “pogo pins”. The “pogo pins” are micro spring loaded pins that punch through the MEMS structure to contact the large pads on the chip.

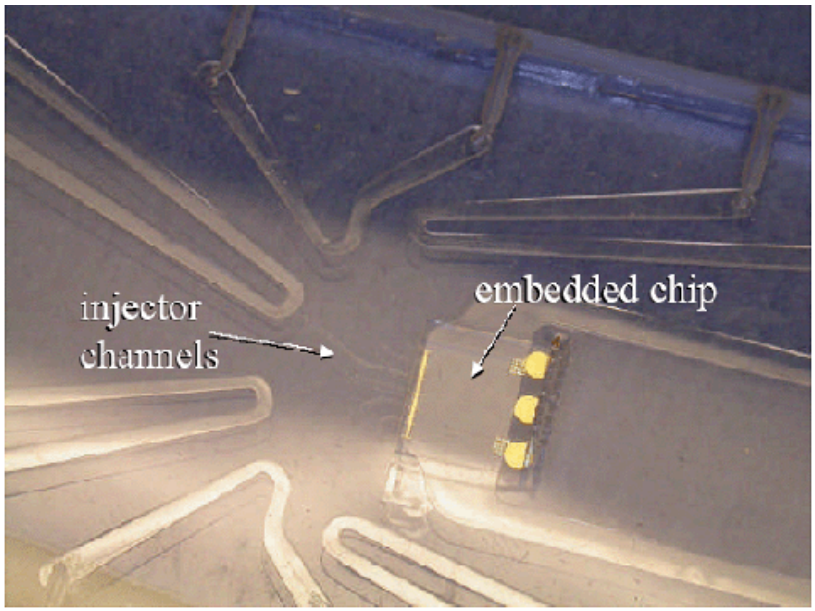

Figure 2-10 Close-up picture of the MEMS fluidic cartridge showing the injector channels chamber region, injection electrodes and vertical contact pogo pins [11]

2.3.6.2.Prototype Benchtop Test Assembly

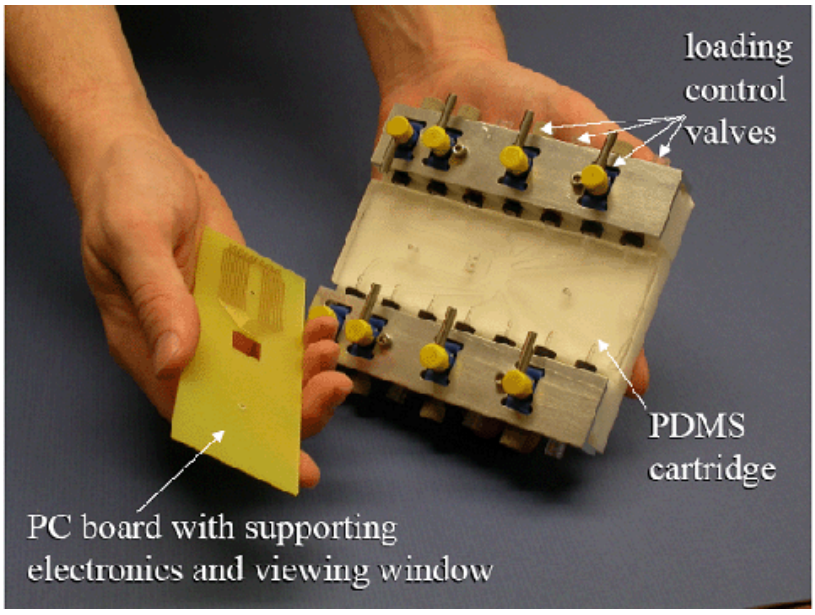

Figure 2-11 Photo of the entire PFP assembly [11]

The prototype benchtop test assembly for the PFP is shown in Figure 2-11. It is composed of the MEMS fluidic cartridge with the location for the embedded electronics chip, a base plate with fluid input ports and loading control valves and a PC board with the supporting electronics needed to power the chip and interface it to the PDA controller.

In the proposed prototype benchtop assembly, the MEMS fluidic cartridge with the PFP IC is placed in the housing between the loading control valve ports. The PC board with supporting electronics mounts on top of the MEMS cartridge and attaches to the vertical pogo-pins that contact the chip. The PC board also has a viewing window for chamber observation. Currently, the method of monitoring the action inside the MEMS chamber is by using a microscope and watching the PFP surface through the viewing window. In the prototype benchtop test version, an automated optical system is used to detect fluorescence of certain dyes.

2.3.7. PFP Interface and Control

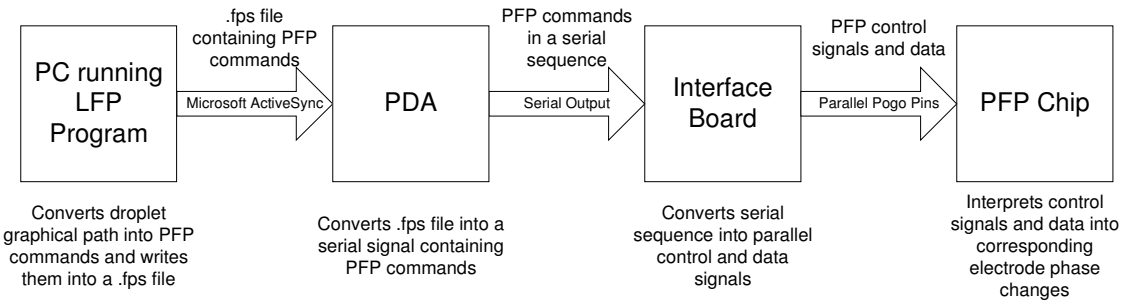

Figure 2-12 High level interface of the PFP IC

The high-level interface and control system for the PFP IC is developed by Lynntech and a block diagram of the components and data path are shown in Figure 2-12. The interface system allows the user to graphically program the desired droplet movement path that is downloaded onto a PDA and translated through a series of stages into sequential phase state changes of the PFP IC electrode array. One of the goals of the interface is to allow the use of a PDA that can store the desired droplet path information and be brought into the field with the PFP system.

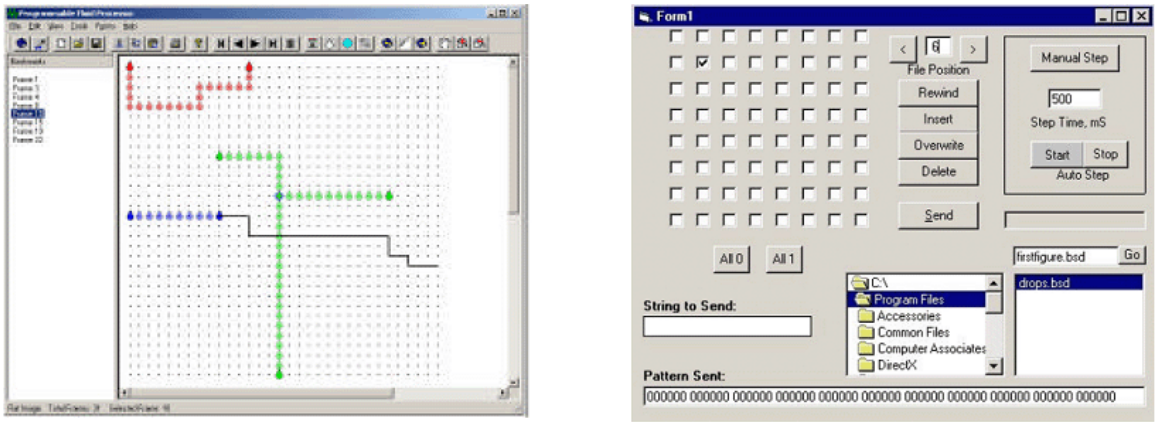

Figure 2-13 Sample screen shots of the LFP program [11,12]

The following explanation of the interface is taken from [13]. To program the droplet movement path, the user inputs the desired droplet movement path using the Lynntech Fluid Processor (LFP) program running on a PC. A sample screen shot of the LPF program is shown in Figure 2-13. The program transforms the droplet graphical path into PFP commands and saves it into an .fps file format. Then, using Microsoft ActiveSync, the .fps file is downloaded from the PC to the PDA. Because the PDA has only one serial output, the commands from the .fps file are transformed into a serial data string containing the PFP commands and data sequences that is then sent to an interface board.

The interface board stores the PFP commands from the PDA into a buffer and then translates them into the corresponding PFP IC control signals and data sequences. The interface board is designed to drive the PFP IC's multiple control lines and sends the PFP commands into the chip through the pogo pins appropriately. Finally, the PFP IC translates the commands from the pogo pins into phase state changes on the electrode array.

2.4. Chapter 2 Summary

This chapter gives a basic understanding of the PFP system in terms of the project goals, specifications and implementation. The motivation for the PFP comes from its potential use in many fields as a robust, portable fluidic analysis system. The mechanism used for droplet movement is based on an effect called dielectrophoresis, in which inhomogeneous fields are used to exploit the dielectric properties of polarizable liquids, generating forces that can move a fluid droplet through a suspending medium. The PFP architecture utilizes an electrode array that produces individually phase-programmable high voltage signals that can be configured to generate potential differences between electrodes and thus the inhomogeneous electric fields that cause dielectrophoresis. Injection of fluids into the PFP system is performed by a combination of forces from both the injector reservoir pressure and the voltage between the injector tip and the droplet collecting electrode. The use of DEP to assist in the injection of fluids establishes a high degree of control of fluid into the MEMS chamber using the same communications circuitry that programs the array. The PFP prototype system uses the PFP1K chip in combination with the MEMS fluidic chamber and vertical pogo pins that route the control signals of PFP1K

to its interface hardware. The PFP system is operated by programming the movement path for the droplet in specially designed software, which transfers that data to a PDA that can be taken along with the portable prototype system. The PDA serially loads the droplet movement path to the PFP interface board, which translates the sequence into the control and data signals required by the PFP1K chip.

In the next chapter, the breakdown mechanisms of HV SOI transistors are explained and the X-Fab XI10 technology is reviewed. The discussion on the HV SOI technology helps to understand the capabilities of the technology for choosing an appropriate high voltage driver design.

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Chapter 3 Silicon-On-Insulator (SOI) Technology

Chapter 3 discusses high voltage SOI technology and the design of high voltage SOI diodes and laterally diffused MOS transistors (LDMOS) in terms of breakdown voltage mechanisms and the parameters that affect breakdown voltage. Chapter 3 also discusses the capabilities of the X-FAB XI10 high voltage SOI technology.

3.1. Introduction

High voltage CMOS technology using standard bulk fabrication has advanced greatly over the last 25 years. The growing development in high voltage fabrication technology stems from the desire to integrate high power devices with control circuitry onto a single IC chip. The result is a simplified system design by allowing protection, diagnostic and driver functions to be incorporated into the power circuits [1].

High voltage devices are made using one of two major types of technology: junction isolated technology (JI) and dielectrically isolated (DI) technology, which are described next.

3.1.1. Types of High Voltage Technology

Junction Isolation (JI) Technology

In junction isolation (JI) technology, the devices in an integrated circuit are separated or electrically isolated from each other using reversed biased P-N junctions [2]. Standard

bulk technology is a commonly used JI technology and high voltage processes in standard bulk have been used for many years.

The advantages of high voltage bulk technology are that very high breakdown voltages up to 1200V can be achieved [3]. However, high voltage bulk technology suffers from limitations due to its shared substrate such as high leakage currents, parasitic bipolar components, increased parasitic capacitances and interference between active devices or circuits built on the same integrated chip [4].

Dielectric Isolation (DI) Technology

One solution to the problems with high voltage JI technology is the use of dielectrically-isolated (DI) devices. In DI technology, the devices in an integrated circuit are electrically isolated from each other by an insulator [2].

Early forms of DI technology involved the isolation of bipolar transistors by surrounding them individually with silicon dioxide. The silicon-on-insulator (SOI) technology like that used in the PFP IC is a type of DI technology in which devices in thin silicon islands are built on top of a buried oxide (BOX) that prevents coupling between the devices through the substrate.

3.1.2. Advantages and Disadvantages of High Voltage SOI Technology

The electrical isolation between devices of a DI technology is superior to that of a JI technology due to the buried oxide between the active silicon layer and the silicon

substrate. As a result, substrate leakage currents, latch-up, surface leakage and interference due to coupling between high and low voltage devices are all theoretically eliminated [5, 6]. The improved electrical isolation benefits the PFP IC by allowing the integration of the CMOS logic circuitry and the high voltage drivers on the same substrate, thereby making efficient use of area and allowing the realization of an array of on-chip programmable high voltage drivers.

SOI devices can be perfectly isolated in the vertical direction by the buried oxide and in the lateral direction by techniques such as local oxidation of silicon (LOCOS), mesa etching and trenches [4]. These three lateral techniques are all similar in principle but differ in processing method. In LOCOS, devices residing on different silicon islands are covered by a silicon nitride mask while a localized pad of oxide is grown by thermal oxidation from the buried oxide on up, electrically isolating the devices. The two silicon islands separated by the LOCOS oxide are shown in Figure 3-1a. In MESA etching, channels are etched away down to the buried oxide between devices as to create silicon islands on which the devices reside, unconnected to their neighbors. Figure 3-1b shows the separation of the devices by mesas resulting from the etching of the silicon layer. In trench isolation, trenches are formed by etching the silicon down to the buried oxide, similar to MESA etching, but an oxide is deposited in place of the etched trench, and is not thermally grown like in LOCOS isolation [7]. The trench structure is shown in Figure 3-1c.

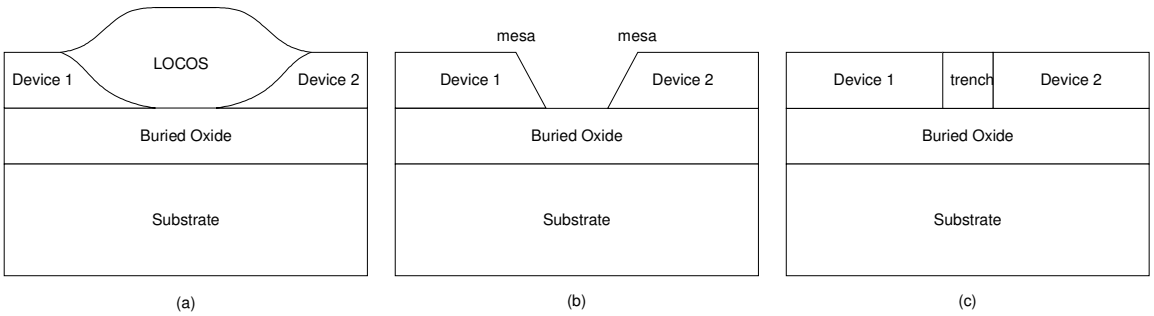

Figure 3-1 Isolation techniques for SOI devices [4] (a) LOCOS isolation (b) mesa etching and (c) trench structures

Despite improved electrical isolation, high voltage SOI devices have a lower breakdown voltage compared to high voltage bulk devices. Breakdown voltages as high as 700V have been realized in SOI [6], but this is still much less than in bulk. The breakdown voltage is limited by the confined electric field distribution resulting from the presence of the buried oxide, which is a major topic of discussion in this chapter.

In this chapter, first the SOI LDMOS will be introduced and the various possible breakdown voltages of the device will be discussed. The drain-to-source breakdown voltage of the transistor will be identified as the performance parameter that sets the breakdown voltage of the transistor. Next, the redistributed surface field (RESURF) concept, a two-dimensional effect that occurs in high voltage diodes and transistors that allows a higher achievable breakdown voltage than a one-dimensional PN junction, will be described for both bulk and SOI high voltage diodes. Following that, the influence of SOI device properties such as silicon layer length and thickness, buried oxide thickness, implantation dose and backgate voltage on the breakdown voltage will be discussed. Finally, some features of the XFAB XI10 SOI technology used for the PFP IC will be overviewed.

3.2. HV SOI Technology

3.2.1. SOI Laterally Diffused Metal Oxide Semiconductor (LDMOS) Transistors

High voltage SOI LDMOS are commonly used because they are highly compatible with standard processing steps. The SOI N-channel LDMOS transistor structure is shown in Figure 3-2 and is composed of a silicon active layer atop a buried oxide and utilizes an extended silicon region between the N drain and the P channel called the drift region to enhance its breakdown capabilities by allowing the potential contours to traverse a larger distance, reducing the electric field in the silicon layer. The implementation of a drift region is used in both bulk and SOI high voltage diodes and transistors.

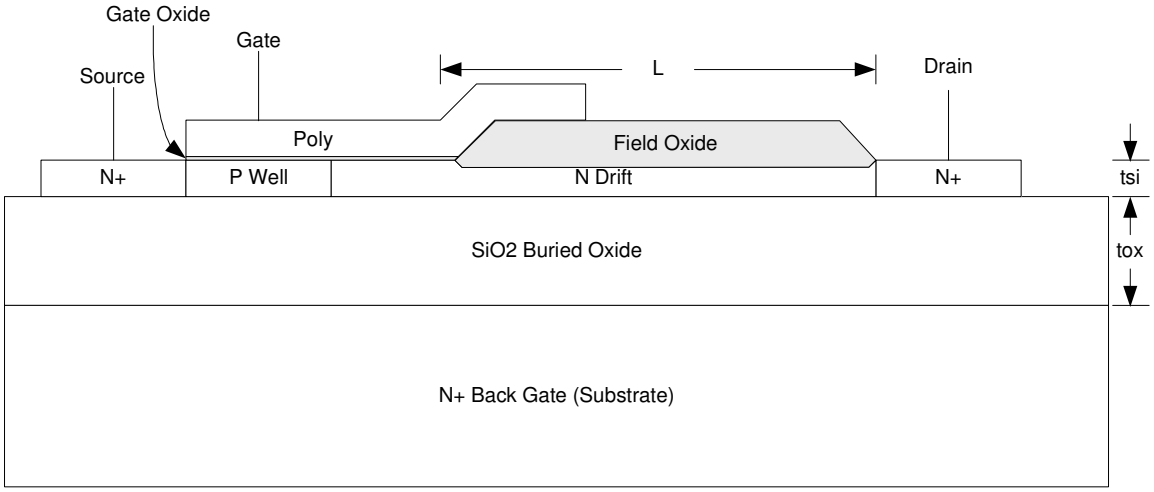

Figure 3-2 Structure of the SOI N-channel LDMOS transistor [4,8,9]

During operation of an N-channel LDMOS (LDNMOS), when the source and substrate are grounded and a voltage greater than the threshold voltage is applied between the gate and source, the transistor turns on and a channel is formed in the P well region between the N-type source and N-type drift region.

3.2.2. Definitions of Voltage Limitations in HV Diodes and Transistors

Voltages applied to a device can cause excessive electric fields, which lead to "breakdown". The electric field value at which "breakdown" occurs is called the critical electric field, or Ecrit, and is specific to different types of breakdown. In this section, avalanche breakdown and oxide breakdown due to excessive electric fields are defined and identified as the causes for the voltage limitations of the high voltage SOI transistor. The conditions for gate-source (gs), gate-drain (gd), drain-source (ds), drain-bulk (db) and source-bulk (sb) breakdown in our application of SOI LDMOS transistors will be discussed briefly and the drain-source breakdown will be identified as the primary breakdown of concern during high voltage drain-source operation.

3.2.2.1.Types of Breakdown

Avalanche breakdown

Avalanche breakdown occurs when the electric field in the silicon in a PN junction due to the applied voltage approaches the critical value of silicon and the carriers gather enough energy to collide into silicon atoms, creating new electron hole pairs through impact ionization. The resulting electrons and holes are also capable of creating more electron hole pairs from silicon atoms. This positive feedback reaction causes excessive charge transport resulting in an abrupt reverse bias leakage current. In a reversed bias PN junction, the avalanche effect is characterized by a multiplication factor equal to the ratio of current flow when impact ionization is present over the current flow when impact ionization is absent [10]. The avalanche multiplication factor is determined by the

applied voltage of the device, the junction breakdown voltage, and the impurity concentration [5].

Oxide breakdown

Similarly, if the electric field in the oxide becomes too high, oxide breakdown can occur, resulting is current flow between areas intended to be isolated by the oxide. Oxide breakdown occurs due to traps in the oxide, which can surface due to manufacturing imperfections or excessive applied voltages and electric fields [11,12]. For example, according to [11,12], in gate oxide breakdown, when the electric field in the gate oxide is too high, electrons in the channel tunnel through the gate oxide to the gate. Each of these electrons can collide with a silicon atom in the gate (assuming a polysilicon gate material) and transfer its kinetic energy to another electron of that atom. That electron is sent to the conduction band of the silicon atom, giving rise to a hole, which then tunnels back into the gate oxide, creating a trap. Holes in the oxide increase the gate current density by hole-induced trap generation. As a result, more high energy electrons from the channel are allowed to tunnel through the oxide and enter the gate, generating more holes to tunnel into the oxide. This process continues until there are enough traps to form a conduction path from the gate to the channel. This type of breakdown is called soft breakdown and may not affect transistor performance in the on-state but may contribute considerable off-state gate current. The conduction leads to heat and the heat leads to thermal damage, which leads to more conduction. Eventually, this positive feedback process causes the silicon in the breakdown path to melt, releasing oxygen, and forming a

silicon filament from the gate to the channel. This stage of breakdown is called hard breakdown.

Avalanche and oxide breakdown in SOI devices

In a high voltage bulk transistor, avalanche breakdown can occur in the horizontal direction between the N-type drift/drain region and the P-type channel region and in the vertical direction between the N-type drift/drain region and the P-type substrate. For an SOI device, like the bulk device, avalanche breakdown can occur in the silicon between the N-type drift/drain region and the P-type channel region. However, unlike bulk, the active silicon layer in an SOI device interfaces with a buried oxide rather than a P-type substrate. In this case, the silicon dioxide buried oxide can be treated like an undoped silicon layer as far as Poisson's equation is concerned [13] and the SOI structure still retains a vertical breakdown path. If the drain-bulk voltage is excessive, avalanche breakdown can occur in the active silicon along this vertical path near the drain due to the reversed biased silicon/buried oxide junction. Horizontal and vertical breakdown both cause excessive carriers in the active silicon resulting in an undesired avalanche current between the source and the drain.

Theoretically, if the electric field is sufficiently high, buried oxide breakdown can occur, creating a current path between the active silicon layer and the substrate. However, this is less likely since vertical avalanche breakdown near or below the drain usually dominates the breakdown voltage in an SOI device. The details of the breakdown voltage in the SOI transistor are discussed in following sections.

3.2.2.2.Determining the Breakdown Voltage of HV Devices

The breakdown voltage of a diode is determined by grounding the anode and substrate and sweeping the cathode voltage until a reverse bias current is observed between the anode and the cathode. The reverse bias voltage at which the current surge occurs is the breakdown voltage. Similarly, the breakdown voltage of a transistor is determined by grounding the gate, source and substrate and sweeping the drain voltage until current is observed between the source and the drain. Due to their similar breakdown mechanisms, discussions on the breakdown voltage of the diode and transistors will be used interchangeably.

3.2.2.3.Breakdown Voltage of HV SOI Diodes and Transistors

High voltage diodes and transistors are designed to handle large voltages across its drain and source terminals. For a high voltage diode, the high voltage is applied across its anode and cathode terminals. For a high voltage transistor, the high voltage is applied between the source and drain contacts. Here, the possible breakdown voltages for the SOI LDMOS are briefly discussed.

Gate-source breakdown for the LDMOS is similar to that of any standard MOS transistor and occurs when the voltage difference between the gate and the source is too high, generating a high electric field that breaks down the gate oxide, which creates a conductive path between the gate and the channel. In a digital circuit, the source of an NMOS is tied to ground and the gate voltage is switched between high and low supply

levels. Limiting the gate-to-source voltage to a standard 5V should ensure that transistor is turned on while preventing gate oxide breakdown due to excessive gate-to-source voltage.

Gate-drain breakdown through the gate oxide requires a high electric field across the oxide due to the gate and drain bias. This is unlikely in the LDMOS transistor, because of the extended drain drift region, which allows the high voltage from the drain to gradually decrease towards the source. The high voltage transistor is designed such that much of the high voltage applied to the drain dissipates over the drift region and is low by the time it reaches the gate. Therefore a high electric field across the gate oxide due to a gate-drain voltage difference is not likely, because the drain voltage does not closely affect the voltage under the gate oxide.

In an LDNMOS, when the drain-to-source voltage is too high, avalanche breakdown can occur along the horizontal direction between the P channel region and the N-type drift region. This mechanism is found in both SOI and bulk LDMOS transistors. The resulting carriers cause an avalanche current between the source and the drain. The drain-to-source breakdown is important, because it characterizes a device's drain-source voltage capability and is the main breakdown of interest.

In an SOI LDNMOS transistor, since both the source and the substrate are grounded, increasing the drain-source voltage also results in an increased drain-bulk voltage, which can cause avalanche breakdown in the vertical direction between the N-type silicon layer

and the buried oxide near the drain. While the buried oxide is not a P-type silicon material, it can be treated as an undoped silicon region [13] and PN junction breakdown can occur between the N drift region and the buried oxide. The resulting carriers will then cause an abrupt drain-source current similar to that found during horizontal drift-channel PN junction breakdown. In fact, the breakdown voltage of high voltage lateral SOI devices is usually dominated by this vertical avalanche breakdown, an effect due to the presence of the buried oxide. Also, if the electric field in the vertical direction due to the drain-bulk voltage is very high, it is possible that the oxide breakdown occur in the buried oxide, allowing current to flow between the drain and the bulk. However, this would require an electric field in the buried oxide exceeding around 600V/um [6]. Breakdown in the silicon layer is much more likely to occur first.

If the source-bulk voltage is nonzero, source-bulk breakdown may occur in the vertical direction similar to drain-bulk breakdown. However, for SOI LDNMOS transistors, breakdown due to the source-bulk voltage is not likely to happen during normal operation because both the substrate and the source are usually grounded in the SOI process. Source-bulk breakdown will occur in a P-type SOI LDMOS (LDPMOS), where the source is tied to the positive supply and the substrate is tied to ground, creating a high electric field in the vertical direction near the source of the transistor.

3.2.3. High Voltage RESURF Devices

The RESURF concept was introduced by [14] in 1980 for bulk high voltage devices and extended for dielectrically isolated devices by [15] in 1991, heavily impacting the design

of high voltage diodes and transistors. The RESURF concept describes how a two-dimensional high-voltage diode or transistor can achieve a breakdown voltage higher than that of a one-dimensional PN junction. RESURF is commonly explained using a diode example and will be explained for both a bulk lateral diode and an SOI lateral diode in this section.

3.2.3.1.High Voltage Bulk Diode Explanation

Consider the bulk high voltage diode in Figure 3-3. The anode is the P+ diffusion to the left, the cathode is the N+ diffusion to the right, the substrate is P-type and the drift region is an N-type epitaxial layer. The length of the drift region, L, and the width of the depletion region, W, are shown.

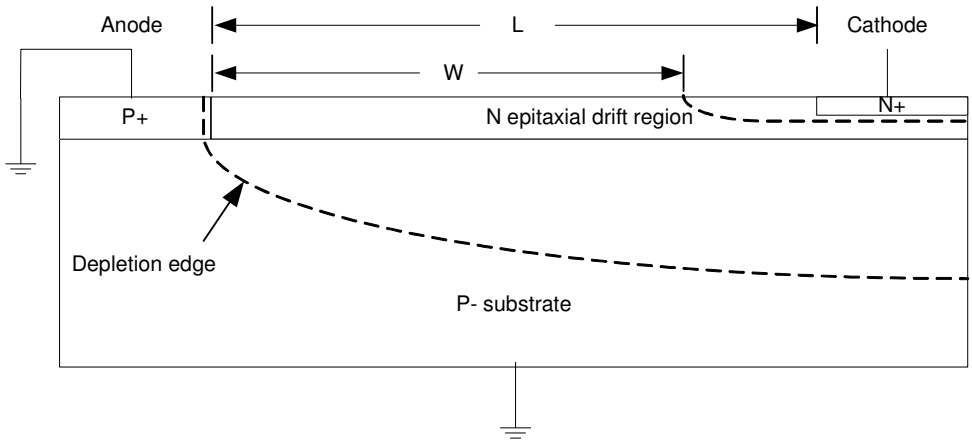

Figure 3-3 Structure of a high voltage bulk diode [6,14]

In the bulk high voltage diode, there are two PN junctions, a lateral PN junction composed of the P+ anode and the N drift region and a vertical PN junction composed of the P substrate and the N drift region. The lateral PN junction line runs vertically, while the vertical PN junction line runs horizontally. The substrate and anode are both

grounded. When a positive voltage is applied to the cathode, reverse biasing the diode, each PN junction creates a depletion region. The lateral PN junction creates a depletion region from the anode to the cathode, while the vertical PN junction creates a depletion region from the drift region into the substrate. The two depletion regions overlap and create a combined depletion region with a width larger than that of a one-dimensional PN junction as bounded by the dotted lines in Figure 3-3. Since the potential variations can only occur within the depletion region, the wider depletion region allows a larger volume for the potential to vary between the anode and cathode. The voltage at the surface is distributed over a wider depletion region, reducing the horizontal electric field along the drift region and allowing a higher applied voltage before avalanche breakdown. Breakdown in the vertical direction is usually neglected because the large depletion region into the relatively thick substrate allows for a potential distribution over more silicon volume and does not limit the device breakdown [4].

A simulation of the potential contours in a high voltage bulk diode is shown in Figure 3-4a [4]. The depletion region extends well into the substrate where a distributed, gradual variation of voltage from the cathode is sustained. With high voltage originating at the cathode terminal, the electric field is evenly distributed in both the lateral direction along the epitaxial layer surface as well as in the vertical direction into the substrate.

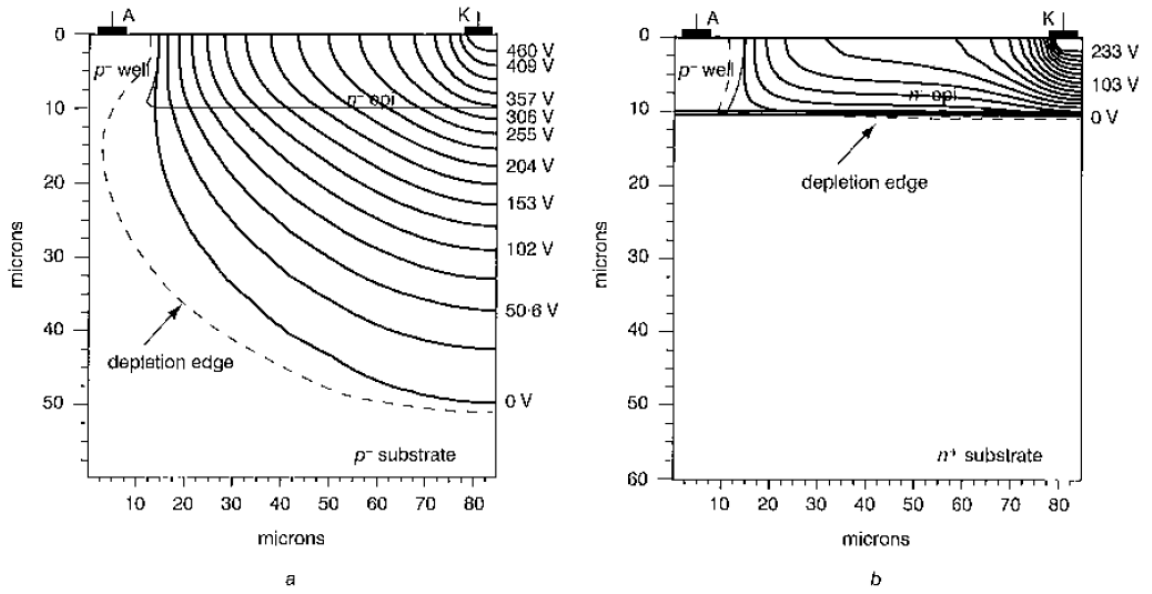

Figure 3-4 Potential contours in (a) a bulk diode and (b) a SOI diode under high voltage operation [4]

3.2.3.2.High Voltage SOI Diode Explanation

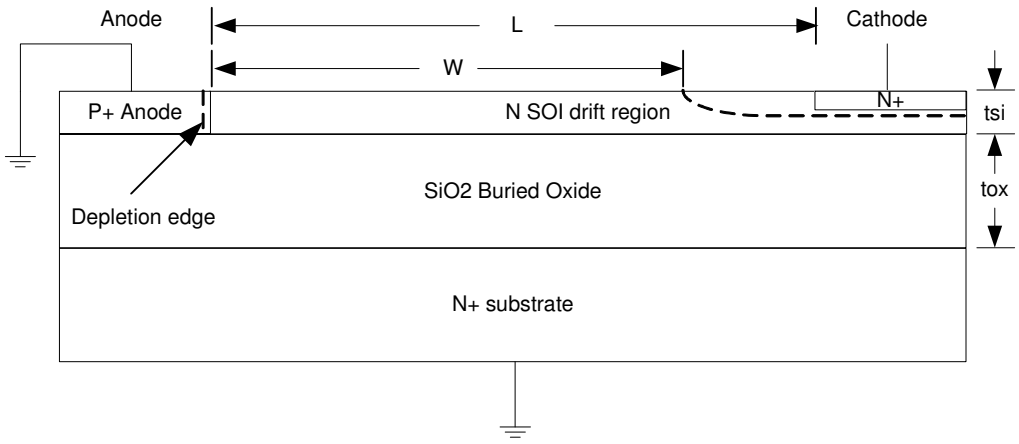

Figure 3-5 High voltage SOI diode [4, 6]

Now consider the SOI high voltage diode in Figure 3-5. It is similarly composed of a P-type anode, N-type drift region and N-type cathode, and like the bulk diode, has a lateral PN junction with a vertically-running junction line. When a reverse bias is applied to the SOI diode, with the substrate and anode connected to ground, a depletion region created by the lateral PN junction under the influence of the buried oxide voltage depletes much of the silicon layer as shown in Figure 3-5. The result is a lateral depletion of

width W that reduces the horizontal component of the electric field. In the vertical direction, however, an oxide layer composed of silicon dioxide intervenes between the active silicon layer and the N-type substrate. The cathode, drift region, buried oxide and substrate form a MOS capacitor and an inversion layer forms at the junction between the buried oxide and the substrate, preventing the depletion region and the electric field from extending into the substrate [15]. A simulation of the potential contours of a high voltage SOI diode at breakdown is shown in Figure 3-4b. Very little of the substrate is depleted, keeping most of it at ground potential and the potential contours originating from the cathode are confined to the silicon area and the buried oxide underneath it. The relatively thin buried oxide supports the entire or a large fraction of the potential drop across it as shown in Figure 3-4b [4]. Due to the high electric field and small vertical distance close to the cathode, the breakdown location is usually dominated by the vertical path rather than the horizontal path but can shift based on the properties of the silicon and buried oxide layers which is discussed in Chapter 3.2.4.

3.2.4. Properties Influencing the Breakdown Voltage of HV SOI Lateral Devices

This section discusses the breakdown voltage and mechanisms of the SOI high voltage devices with respect to the drift region length, drift region thickness, buried oxide thickness, implantation dose and backgate/substrate voltage parameters. First, using a high voltage SOI diode as an example, the two breakdown paths, the horizontal path along the silicon surface and the vertical path near the drain edge, will be identified. Then the ideal breakdown voltage set by the horizontal breakdown path and its relationship to the drift region length will be described. After the ideal breakdown is

established, the effects of the vertical breakdown path will be considered and the subsequent reduction of the breakdown voltage from that ideal will be described. This deviation from the ideal horizontal breakdown voltage created by the vertical breakdown path is caused by limitations due to the silicon and buried oxide thickness.

3.2.4.1.Horizontal and vertical breakdown path of high voltage SOI devices

High voltage SOI diodes and transistors using a thin silicon layer and thick buried oxide have two breakdown paths: one is the horizontal PN junction path along the top or bottom surface of the drift layer, the other is the vertical path at the drain/cathode edge of the depletion region [9]. The path that breaks down at a lower voltage sets the drain to source avalanche breakdown voltage since both the drain and substrate are grounded. The breakdown voltages of the two paths depend on certain properties of the high voltage device, which will be discussed next.

In a bulk device, the horizontal path has a lower breakdown voltage than the vertical path and sets the breakdown voltage of the device. However in an SOI device, the vertical breakdown path has a lower breakdown voltage than its horizontal breakdown path and sets the breakdown of the device. Since the horizontal breakdown mechanism found in SOI devices is the same found in bulk devices, it is considered the ideal breakdown mechanism for the SOI device. However, in most cases, vertical breakdown in the SOI device occurs before horizontal breakdown and sets the SOI device's actual breakdown voltage. First, ignoring the vertical path, the horizontal breakdown path and its relationship to variations in the drift region length will be discussed. The vertical path

can be neglected, so long as the silicon layer is assumed to be very thin and the buried oxide is very thick [9]. After the ideal horizontal breakdown voltage is established, effects of the vertical path resulting from non-optimal SOI and buried oxide thickness will be considered and how they limit the breakdown voltage from the ideal will be explained.

3.2.4.2.Optimization of the Electric Field Along the Horizontal Breakdown Path

To maximize the horizontal breakdown voltage of a RESURF SOI device, the horizontal electric field within the silicon area must be evenly distributed within the silicon volume to minimize ionization along the horizontal path [6,9]. Improving the horizontal electric field distribution in the device is done primarily by extending the drift length for a given drain voltage.

Drift length

In a high voltage SOI LDMOS, the drift region length identified by L in Figure 3-2 is measured from the edge of the gate electrode to the edge of the drain region, and in a high voltage SOI diode, it is measured from the edge of the anode to the edge of the cathode as identified by L in Figure 3-5.

Increasing the drift region relaxes the electric field in the silicon by allowing the potential lines to traverse a larger distance between the N and P regions. By relaxing the electric field in this way, a higher horizontal breakdown voltage can be achieved. The horizontal breakdown voltage increases almost linearly with increasing drift region length [9] and so

very high horizontal breakdown voltages can be achieved simply by extending the drift region.

3.2.4.3.Optimization of the Electric Field Along the Vertical Breakdown Path

However, the advantages of extending the drift region length are limited by the influence of the vertical breakdown path. At small drift lengths, the breakdown voltage is dominated by the horizontal path and uniform distribution of the lateral electric field is critical. However, as the drift length is increased, the breakdown path responsible for the breakdown voltage shifts from the horizontal path to the vertical path [9].

When the vertical path is considered, the breakdown voltage saturates and no longer increases linearly with increasing the drift length [9,15]. It levels off at a voltage determined by the vertical breakdown path at the drain junction (or near the cathode in high voltage diodes), which is decided by the thickness of the silicon layer and buried oxide [9,15].

As the horizontal electric field is uniform and the drift length optimized, the vertical electric field will vary across the thickness of the SOI layer if the vertical doping concentration in the drift region is uniform [9]. Since the entire substrate is at equipotential, the vertical distance for the potential contours to expand from the drain/cathode is limited to the silicon layer thickness plus the buried oxide thickness. Therefore, the vertical electric field close to the drain/cathode is very high, and sets the breakdown voltage of the device. The vertical breakdown voltage can be expressed by:

$$BV(vertical)=(tsi/2 + 3tox)Ey(W,tsi), \quad (1)$$

where tsi is the silicon thickness, tox is the buried oxide thickness, Ey is the critical field in the vertical direction as a function of depletion width W, and 3 is substituted for the ratio of dielectric constants of the silicon and oxide, Ks/Kox=3 [6]. The thickness parameters are labeled for the SOI lateral transistors and diodes in Figures 3-2 and 3-5, respectively. The effects of the layer thicknesses on the breakdown voltage will be explained next.

Drift layer thickness

Earlier studies on the effects of the drift layer thickness on breakdown voltage of SOI devices determined that the breakdown voltage increases with increasing silicon layer thickness [15] since the electric field in the vertical direction decreases with increasing silicon layer thickness [1]. This is only valid for a larger silicon thickness and in fact, below a certain value, breakdown voltage actually increases with decreasing silicon thickness [6].

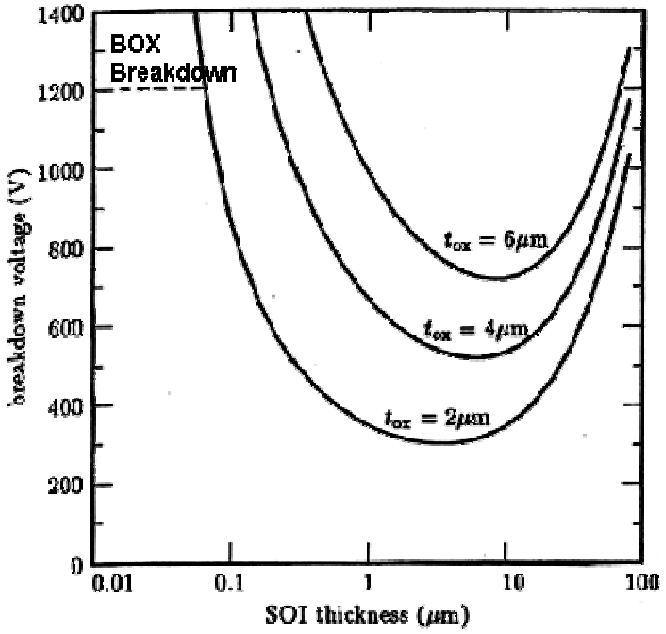

Figure 3-6 Theoretical breakdown voltage versus SOI thickness for buried oxide thickness tox=2um, 4um, 6um. This graph is valid in the limit where the lateral depletion width is large. The dashed line corresponds to dielectric breakdown of the 2um thick buried oxide. [6]

According to [6], the breakdown voltage as a function of the silicon thickness actually forms a U shape and is shown in Figure 3-6 for tox=2um, 4um and 6um. From equation (1) it can be seen that increases in the silicon thickness will directly increase the vertical breakdown voltage. However, the critical electric field in the vertical direction, Ey, is also a function of the silicon thickness and increases for decreasing tsi according to the ionization integral derived in [6], which then allows for a higher realizable breakdown voltage. For a given electric field and oxide thickness, the breakdown voltage increases with increasing silicon thickness above about 10um and increases with decreasing silicon thickness below about 1um [6,8].

Buried oxide (BOX) thickness

In the ideal case where the horizontal breakdown dominates, the vertical breakdown can be ignored if the buried oxide is very thick allowing the vertical electric field to distribute

over a larger area. However, if the buried oxide is too thin, it does not contribute much vertical distance for the potential contours to extend into and the electric field is confined along the vertical path from drain to substrate over a distance set primarily by the thickness of the silicon layer. In turn, the vertical electric field will exceed the critical electric field of the silicon layer at a lower applied voltage than the ideal horizontal breakdown case. For example, the breakdown voltage saturates by vertical breakdown at around 500V and 680V at buried oxide thicknesses of around 1.2um and 1.6um, respectively, with a silicon layer thickness of 0.1um [9].

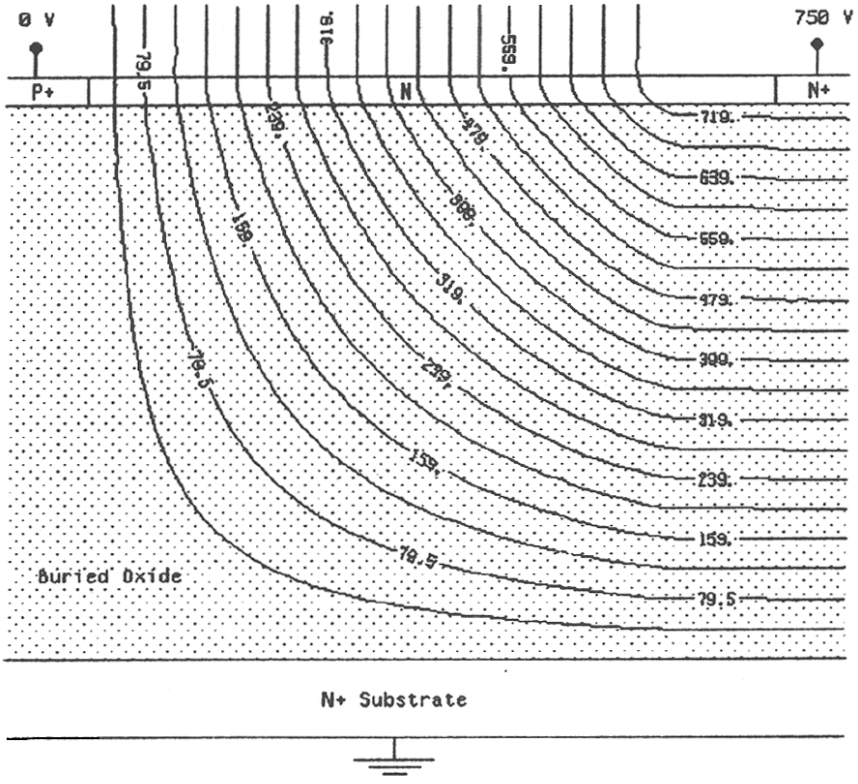

Figure 3-7 Two-dimensional off-state numerical simulation of the SOI diode of Figure 3-2 with ts=0.1um, tox=2um, and L=70um (not to scale). Potential contours are shown for reverse bias breakdown voltage of 750V as determined by numerical evaluation of the ionization integrals [6].

Increasing the buried oxide thickness can give a higher breakdown voltage because the potential contours from the drain are allowed to spread into the oxide, lessening the vertical electric field in the silicon layer [1,6]. A numerical simulation of a high voltage SOI diode optimized to provide both uniform lateral and vertical E field distribution is shown in Figure 3-7 [6]. The diode has a 750V breakdown with a drift length of 70um to provide uniform horizontal electric field distribution and a buried oxide thickness of 2um to provide uniform vertical electric field distribution. When the buried oxide is thick, the breakdown voltage approaches the ideal case and therefore it is difficult to determine whether the breakdown is set by the ideal horizontal path or the by the vertical path whose breakdown voltage has been increased by the thicker oxide. According to [9], saturation of the breakdown voltage due to vertical breakdown is eliminated for a buried oxide thickness of 4.4um and silicon thickness of 0.1um and the horizontal path sets the breakdown voltage.

Equation (1) verifies that the breakdown voltage increases proportionally with the buried oxide thickness. However, unlike the silicon thickness, Ey is not a function of the buried oxide thickness [6]. Although increasing the buried oxide thickness seems like a simple solution to increasing the breakdown voltage, is limited by practical processing considerations.

3.2.4.4.Implantation Dose

Since the RESURF concept relies on the coupling of charge in the drift region to the substrate through the buried oxide layer, changing the drift charge by implant dose can

alter the total charge in the drift region and consequently, the electric field distribution in the silicon. According to the high voltage SOI diode discussion in [15], a high implant dose will cause an electric field peak at the anode side of the drift region, while a low implant dose will cause an electric field peak at the cathode side. A high electric field at either of these places will disrupt a uniform electric field distribution and lead to a lower breakdown. Therefore, it is important to choose a doping such that the electric field is evenly distributed to achieve a high breakdown voltage [15]. One suggestion to improve the uniformity of the lateral electric field is to linearly grade the doping concentration along the drift region to optimize the RESURF condition [4].

3.2.4.5.Substrate Voltage

This section discusses the effect of the backgate or substrate voltage on the drain to source breakdown voltage of the high voltage SOI device. As established previously, vertical breakdown occurs in an SOI device near the drain/cathode due to the buried oxide, which causes an inversion layer to form at the top of the substrate preventing depletion and potential contours from extending into it. The entire voltage applied to the drain/cathode varies between the drain/cathode and the top of the substrate which imposes a high electric field along that vertical path as shown in Figure 3-8a for a high voltage SOI diode example.

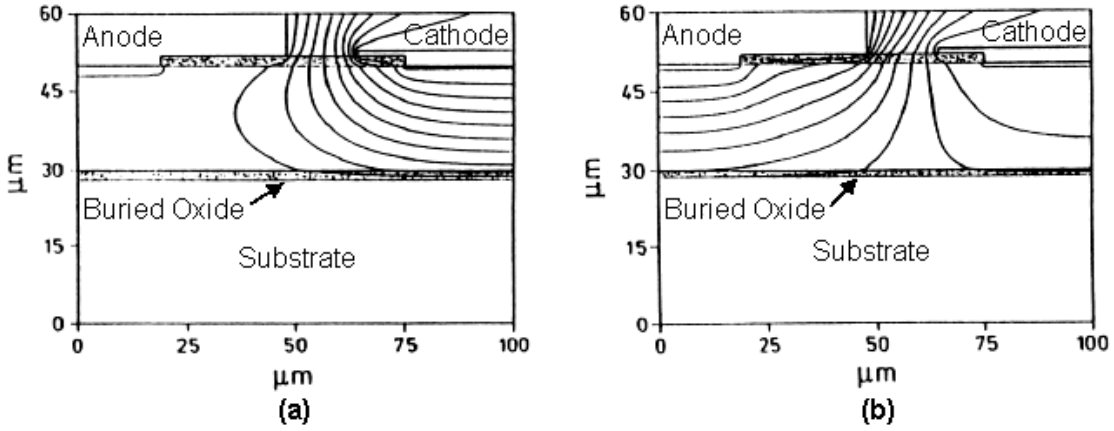

Figure 3-8 Simulated potential distribution of a high voltage SOI diode with (a) Vbackgate=0V, simulated BV= 470V, measured BV=500V and (b) Vbackgate=400V, simulated BV=650V, measured BV=450V [1]

Varying the substrate voltage can change the distribution of the electric field within the drift region and change the location of the vertical breakdown path. With the backgate and anode tied to ground and applying a voltage to the cathode, a high vertical electric field from the cathode to the substrate below is formed as shown in the simulation in Figure 3-8a. Here, the simulated breakdown voltage is about 470V and the measured breakdown voltage is about 500V [1]. No electric field exists between the anode and the substrate because both are at 0V. When the substrate voltage is increased from 0V, a voltage difference and electric field between the anode and substrate is formed, while the voltage difference between the cathode and the substrate decreases. A simulation of the same diode with a backgate voltage of 400V is shown in Figure 3-8b. The simulated breakdown voltage is about 650V while the measured breakdown is about 450V [1]. The measured breakdown voltage actually peaked at about 630V with a backgate voltage of 200V rather than at 400V [1]. As a result, a higher voltage can be applied to the drain before vertical breakdown occurs there. If the substrate voltage is increased even further, a high electric field resulting from a large potential difference between the anode and the

substrate under it may become even larger than that at the cathode end. The vertical electric field near the anode will reach the critical value at a lower voltage than the cathode end and breakdown will occur there first. Thus, changing the substrate voltage redistributes the electric field between the anode and cathode ends and can alter the location of the vertical breakdown, which can lead to reduced breakdown.

3.3. XFAB SOI XI10 Technology

3.3.1. Technology Overview

The information contained in this section regarding the Xfab's XI10 process technology is a combination of publicly available information from the Xfab website [16] and data taken at UC Davis. Details on the XI10 technology cannot be divulged due to a confidentiality restriction.

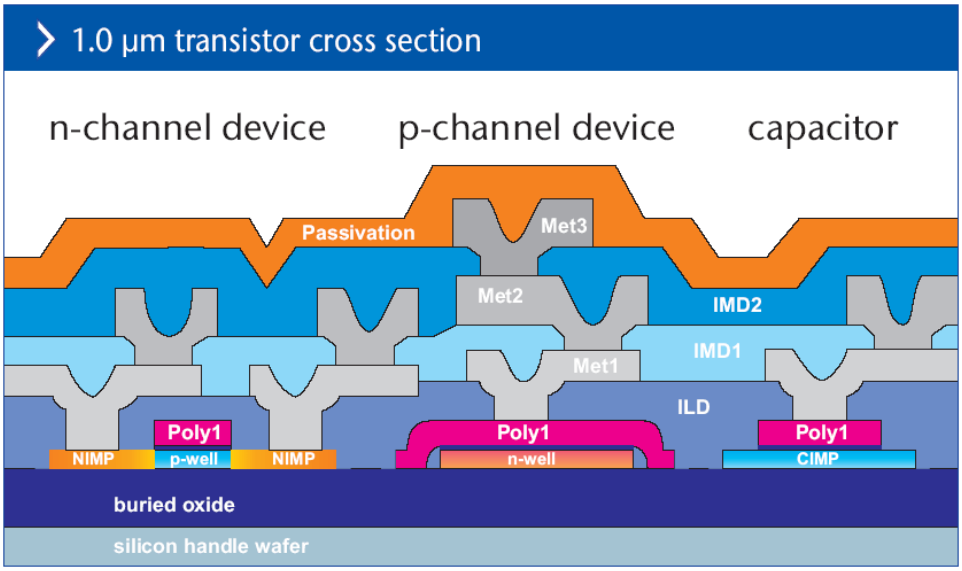

Figure 3-9 Cross section of an n-channel, p-channel device and capacitor in XI10 [16]

Overview

The XFAB XI10 is a 1.0 µm single poly, 3 metal non-fully depleted SOI technology with 1000 nm thick buried oxide, 250 nm thick active silicon layer and 25 nm thick gate oxide [16]. A cross section diagram of the technology is shown in Figure 3-9. During operation of a non-fully depleted or partially-depleted SOI (PDSOI) transistors, the depth of the depletion region is not limited by the depth of the silicon layer and a portion of the body is non-depleted. On the contrary, fully depleted SOI (FDSOI) transistors have depletion depths that extend to the buried oxide, completely depleting the silicon layer. Circuits fabricated in PDSOI technology inherit the benefits of SOI, while preserving the performance characteristics of standard bulk MOS transistors. It is believed that all the transistors in the XI10 technology are partially depleted including the high voltage LDMOS transistors.

The specifications of interest are the threshold voltage and the breakdown voltages of the high voltage transistors and low voltage transistors. The transistor layouts used in the PFP IC are from the XI10 cell library.

High voltage transistor characteristics

The high voltage NMOS transistors in the XI10 cell library are double-diffused mosfets (DMOS) with drift lengths of 3um, 6um and 10um, capable of 70V, 100V, and 130V breakdown, respectively [16]. The breakdown voltage of the high voltage PMOS with drift length of 3um is –60V, but is said to be “undetermined” for the drift lengths of other sizes. The PFP IC uses n-channel DMOS with 10um drift length but not p-channel

DMOS due to their undetermined breakdown voltage. The threshold voltage of the high voltage n-channel DMOS transistors is 1.65V. These threshold voltages (VT) and maximum breakdown voltages (BVMAX) are summarized in Table 3-1.

Table 3-1 Threshold and breakdown characteristics for n-channel and p-channel high voltage DMOS transistors of drift lengths 3um, 6um and 10um [16]

High Voltage SOI-DMOS Transistor Parameters				
Parameter	Drift length	Unit	n-channel	p-channel
VT	All	V	1.65	-1.10
BVMAX	3um	V	70	-60
BVMAX	6um	V	100	tbd
BVMAX	10um	V	130	tbd

5V transistor characteristics

The 5V NMOS and PMOS transistors in XI10 are body tied [16], which means the undepleted region of silicon is grounded and the floating body effects are eliminated [5]. The typical parameters for body-tied 5V SOI n-channel and p-channel MOS transistors with channel width W=6um and channel length L=1um are summarized in Table 3-2. The NMOS threshold voltage is 1.65V while the PMOS threshold voltage is –1.25V [16]. The drain-to-source breakdown voltages (BVDSS) of the n- and p-channel transistors are 12.5V and –12.5V, respectively [16].

Table 3-2 Threshold, current and breakdown characteristics for body-tied n-channel and p-channel 5V SOI transistors with W=6um and L=1um [16]. The current specification is given for H-type transistors with W=6um and L=1um (6x1H) [16].

Typical 5V SOI-CMOS Parameters with channel width W=6um and length L=1um and body tied to ground			
Parameter	Unit	n-channel	p-channel
VT	V	1.65	-1.25
IDS 6x1H	uA	900	-600
BVDSS	V	12.5	-12.5

3.3.2. Measured and Simulated XI10 Device Characteristics

The XI10 technology features high precision BSIM3V3 SOI partially-depleted transistor models for HSPICE, which are used in the simulations of PFP.

Current output performance

The characteristic curves of the drain current, ID, versus the gate-source voltage, VGS, for the 5V n- and p-channel transistors and the high voltage n- and p-channel transistors are shown in Figure 3-10. An HSPICE simulation and an experiment of each transistor in a diode-connected configuration are compared. The HSPICE simulations were performed using the XI10 BSIM3 models and the experimental data were taken from transistors found on fabricated test circuits on the PFP test chips.

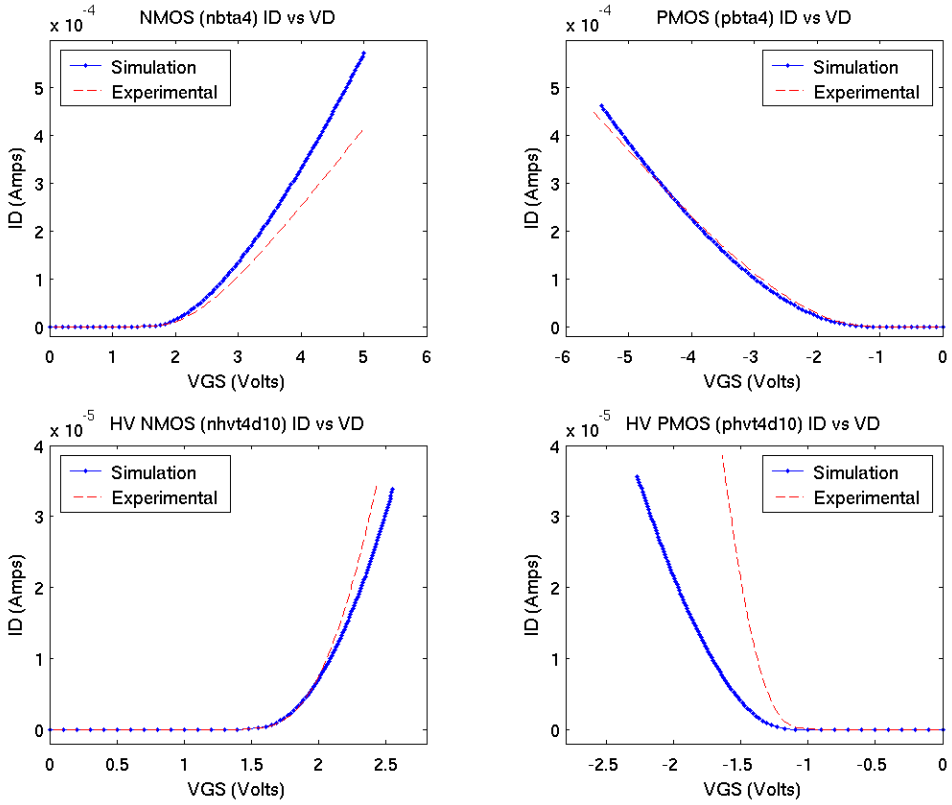

Figure 3-10 Measured and simulated characteristic ID curves as a function of VGS (for VDS = VGS) for NMOS, PMOS, HV NMOS and HV PMOS transistors.

The simulations and measurements show that the models are fairly representative of the performance of the actual transistors. For the low voltage transistors, because they are used in digital circuits that operate at VDD=5V, the simulated and measured current output at VGS=5V are compared. For the 5V NMOS transistor at VGS=5V, the simulation shows a current output of around 565µA while the experimental measurement shows a current output of around 420µA. The tested NMOS transistor seems to produce slightly less current than the model shows, but it is still close. For the 5V PMOS transistor at VGS=5V, the simulation shows a current output of around 385µA while the experimental measurement shows a current output of around 369µA, also showing close agreement.

The high voltage transistor gate voltages are not swept to 5V like the 5V transistors. Instead, the HV transistor output current is compared between the experimental and simulated data at the threshold voltages given by [16]. For the HV n-channel DMOS at a gate voltage VGS=1.65V, the simulation shows a current output of 702nA while the experimental measurement shows a current output of 557nA. At a higher gate voltage of 2.4V, the simulation shows an output of 24.6μA while the experiment shows an output of 32.0μA, showing close agreement. For the HV p-channel DMOS at a gate voltage VGS=-1.10V, the simulation shows a current output of only 28.5nA, but the experimental measurement shows a considerably larger current output of about 328nA. At a higher gate voltage of VGS=-1.6V, the simulation shows an output of 6.53uA while the experimental measurement shows an output of 33.4uA which is also considerable larger. The HV p-channel DMOS current characteristic deviates significantly from the model's output but is not used in the PFP IC design and therefore has no effect on the prototype PFP IC's performance.

Threshold voltage and current gain, K'

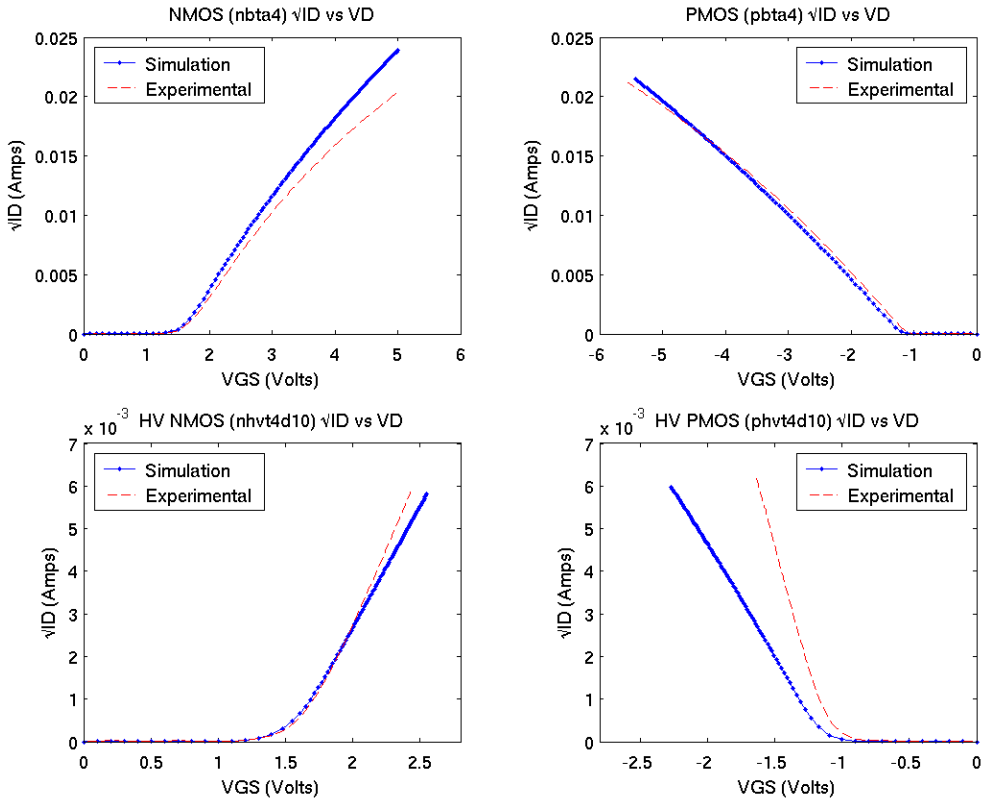

Figure 3-11 sqrt(ID) as a function of VGS (for VDS=VGS) for NMOS, PMOS, HV NMOS and HV PMOS transistors

The square root of the drain current obtained from HSPICE and experimentation are shown in Figure 3-11. From these plots, the modeled and experimental threshold voltage, VTH, and K' of each transistor are approximated by the straight line estimation of the sqrt(ID) curve and its intersection with the VGS axis. The VTH and K' parameters are summarized and compared in Table 3-3. The measured and simulated threshold voltages are close for all the transistors and do not differ by more than 0.1V. The measured K' of the 5V N- and PMOS and the HV NMOS transistors are on the same order of magnitude and are close to the simulated results. However, the measured K' of

the HV PMOS is 0.1337e-3 A/V^2 and much higher than the simulation result of 0.2615e-4 A/V^2.

Table 3-3 Parameters VTH and K' extracted from experimentation and simulation for high and low voltage NMOS and PMOS transistors

Device Name	HSPICE BSIM3SOI Model Simulation		Experimentally measured from PFP test chip circuits	
	VTH	K'	VTH	K'
NBTA4	1.5V	0.4675e-4 A/V^2	1.5V	0.3379e-4 A/V^2
PBTA4	-1.2V	0.2705e-4 A/V^2	-1.1V	0.2445e-4 A/V^2
NHVT4D10	1.52V	0.3070e-4 A/V^2	1.62V	0.5017e-4 A/V^2
PHVT4D10	-1.6V	0.2615e-4 A/V^2	-1.63V	0.1337e-3 A/V^2

3.3.3. High Voltage Limitations Due to SOI Backgate Bias

In the XI10 technology, it is likely that the HV NMOS has maximum breakdown capability when its substrate is tied to 0V and its source-to-bulk voltage is 0V. At higher substrate voltages, the HV NMOS will have a lower breakdown voltage. Similarly, the HV PMOS has maximum breakdown capability when the substrate is tied to the high-voltage 100V supply and its source-to-bulk voltage is 0V. At lower substrate voltages, the HV PMOS will have a lower breakdown voltage. As a result, the HV NMOS and the HV PMOS cannot coexist on the same substrate and both realize maximum breakdown because the substrate is shared and can only be set to a single voltage. If the backgate voltage is compromised, say at 50V, the HV NMOS and HV PMOS may both be able to realize a high breakdown voltage simultaneously, but this voltage will be lower than their individual maximums, because within each transistor, the E field distribution still has been compromised albeit to a lesser degree. Also, the 5V circuits operate on a substrate voltage of 0V and so a 50V backgate may result in unexpected operation.

3.4. Chapter 3 Summary

This chapter introduces high voltage SOI MOS technology and compares its main benefits and drawbacks to high voltage bulk technology, suggesting high voltage SOI technology as a better candidate for a high voltage system on a chip. An overview of the high voltage SOI diode and SOI LDMOS and their breakdown mechanisms is given. The types of breakdown that occur in a high voltage SOI device are described, identifying the drain-source breakdown as the major breakdown voltage of interest. The two-dimensional RESURF concept is summarized and the breakdown mechanism for high voltage bulk and SOI diodes is shown, illustrating the high voltage capability of the SOI high voltage device as well as its lower breakdown voltage compared to bulk. The high voltage capability of a RESURF high voltage SOI device is shown to be governed by two breakdown paths, the horizontal breakdown path and the vertical breakdown path, which are characterized by three main device parameters: the drift region length, the drift layer thickness and the buried oxide thickness. The vertical breakdown path usually dominates the breakdown voltage due to the limitations in silicon and buried oxide thicknesses. Additional parameters that affect the breakdown voltage are the implantation dose and the backgate voltage, both of which can cause a lower breakdown by disrupting the uniform electric distribution in the silicon layer.

Features of the XFAB XI10 Technology related to the breakdown voltage and the threshold voltage of the high and low voltage transistors are overviewed. The current gains and threshold voltages of the transistors are compared between measured data from PFP test chips and HSPICE simulations using the XI10 BSIM3 models. From the

comparison, all of the devices behave according to their HSPICE models except for the high voltage PMOS which is not used in PFP. The effect of the backgate voltage bias on the breakdown voltage of the high voltage NMOS and PMOS transistors is discussed and an explanation given as to why the PMOS are not used in the high voltage digital driver design. A substrate voltage at ground results in a low PMOS breakdown voltage and the NMOS and PMOS cannot realize their maximum breakdown voltages simultaneously on the same substrate biased at a single voltage.

In the next chapter, the PFP1K chip circuitry will be described in terms of the communication and driver circuitry as well as the data buffer design and droplet injection circuitry.

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Chapter 4 Design of the PFP IC Electronics

Chapter 4 describes the PFP IC electronic system design in detail. Here, the overall system operation and the system hardware consisting of the memory elements, driver cells, communications shift register, and decoders are described. The buffer design for intermediate signals is also discussed here along with the DEP assisting injection circuitry.

4.1. Overview of the PFP IC System and Chip

4.1.1. Description of PFP IC Electronics

The Programmable Fluidics Processor Integrated Circuit (PFP IC) consists of 1024 high voltage digital driver cells arranged in a 32-by-32 cell grid array, each capable of producing a 100V peak high-voltage square-wave pulse at its output electrode. The driver cell at each array location converts a 5V square-wave reference signal into a 100V high voltage square-wave output signal and is capable of altering its phase relative to that reference signal. The two possible output signal phase states are 0 degrees and 180 degrees in-phase with the input. The ability to change the phase of the output signals between adjacent array locations is what will allow the dielectrophoretic effect to occur. Fluid droplets present in the MEMS fluidic chamber that will sit atop the PFP IC will experience DEP forces generated by the high voltage electrodes on the chip below.

4.1.2. System components of PFP IC

The PFP IC is composed of the high-voltage electrode driver array and driver array communication circuitry. The high-voltage electrode driver array is composed of identical digital electrode driver cells of 200um square repeated in a two-dimensional grid arrangement, each with a 100um electrode in the center. The digital driver cells used in the array each use a two-stage latch memory element that allows the storage of new phase data while its current phase state is maintained at the output. In turn, digital driver cells can be programmed sequentially with their new phase data and when finished, can simultaneously update their outputs. In addition to the standard driver electronics, circuitry dedicated to assisting droplet injection into the MEMS chamber is connected to the outermost column of electrodes, making them capable of a third, grounded output state. The injection components will be described in more detail in 4.7.

The communication circuitry allows programmability of the array cells from an external control and consists mainly of an 11-bit communications shift register that serially reads in the address and phase data, and two 5-bit address decoders that translate the addresses from the shift register into enable signals for the targeted driver cell within the array. An 11-bit parallel bank of 2-input AND gates (AND2) at the shift register outputs provides control over the propagation of the data to the decoders and the array. Data buffers are placed between the AND2 gates and the array for the phase data line, between the AND2 gates and decoders for the address data, and between the decoders and the array for the row and column lines in order to enhance the driving capability of those intermediate signals to handle large fan-outs.

The PFP IC behaves like a processor in that the droplet movement can be programmed by addressing and modifying the phase state of a cell output through serial address and phase data. In addition, external signals control the data flow and operation of the system in stages.

4.1.3. PFP IC Control and Interface

The PFP IC system is programmable in that the phase output state of each electrode cell element can be configured independently. Each driver can be switched between two states by programming the data bit stored in the cell's 1-bit dual latch memory. The programming of a cell memory requires that the cell memory be enabled and enabling a cell memory requires that the row and column location of the target cell be activated. The array driver cells are individually addressed according to their row and column location by sending the cell addresses into a communications shift register. The standard operation of the PFP IC is controlled by eight external signals and is powered by three supply lines. The injection electronics use two extra external signals, one for the data input of the third state driver cell and one for the injector reference electrode voltage and will be discussed separately in Chapter 4.7. The PFP IC control signals trigger the loading of data into the shift register, the passing of that valid data vector to the decoders that enable the desired array cell, the updating of a target cell's memory and the simultaneous update of the electrode array outputs.

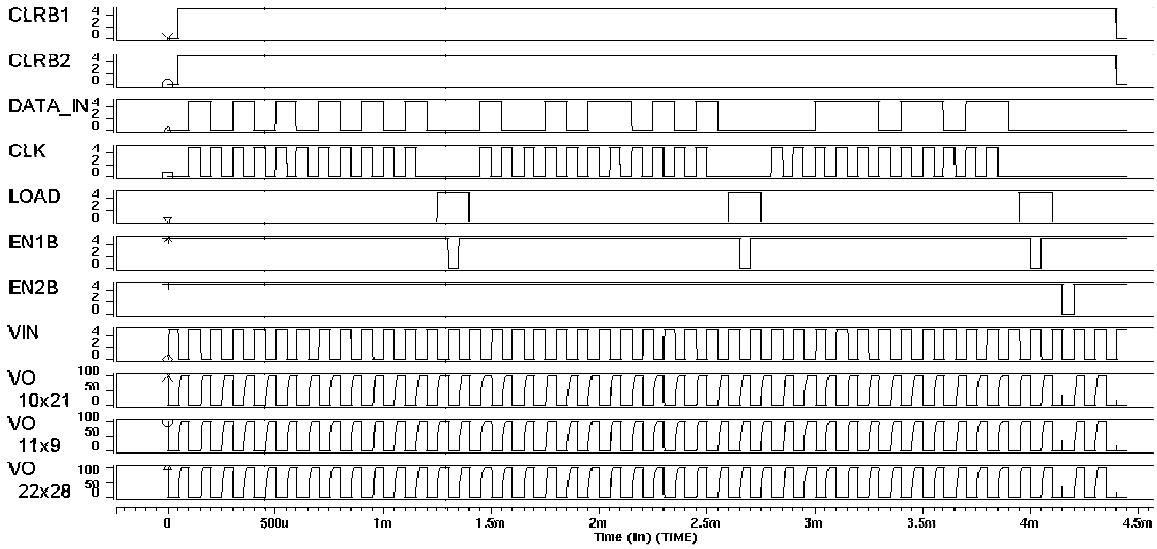


Figure 4-1 Timing diagram of the control signals for the PFP IC operating at 10kHz during three sequential programming cycles followed by a simultaneous array update

A timing diagram of the external signals needed to operate the PFP IC is shown in Figure 4-1. The figure illustrates the control signals issued during the sequential programming of three different cells with their new phase data followed by a simultaneous update of the output at time 4.1s. The three programmed cells shown in Figure 4-1 are (10,21), (11,9) and (22,28).

Table 4-1 Supply, input and control signals for the PFP1K prototype engine

Signal Name	Function
CLRB1	Resets the Shift Register memory
CLRB2	Resets the Driver Cell memories
DATA_IN	Serial input to the shift register for reading the new phase state and addresses
CLK	Shift register enable signal
LOAD	Controls the passing of the valid addresses from the shift register to the decoders and the new phase data from the shift register to the array driver cells.
EN1B	Enables the input latch of the master-slave dual latch of the targeted driver cell
EN2B	Enables the output latch of the master-slave dual latch of the targeted driver cell. Once activated following EN1B, the electrode outputs of all cells are updated with their new phase state memory.
VIN	Serves as a reference signal for the digital driver outputs. The phase of the digital driver outputs will be either 0-degrees or 180-degrees in-phase with VIN depending on the cell's stored data
INJ	Input data to the ground state injection column circuitry
REFINJ	Voltage at the injection reference electrode
V5	Supply voltage for the CMOS logic
V100	Supply voltage for the high voltage output driver
VSS	Ground reference voltage

The signals and their functions are summarized in the Table 4-1. The normal operation of PFP IC is as follows: the user chooses to program the state of a particular cell by inputting the column address, row address and desired phase state into the shift register at the serial input DATA_IN. The shift register reads in a new data bit for every strobe of the CLK signal. Once the data bits are correctly loaded into the shift register, the cell addresses and phase data are passed to the decoders through 11 parallel 2-input AND gates controlled by the LOAD signal. Once passed, the decoders translate the binary addresses and apply a logic high signal to the corresponding row and column lines. Once the row and column lines of the targeted cell are enabled, the memory of the cell at that location can be controlled. This ensures that the enable signals that control the cell memory only affect the targeted cell. At the same time, the phase data bit is sent from the

shift register to the data input lines of all the driver cell memories. When EN1B is pulsed from high to low, the dual latch memory of the targeted cell is enabled and the data is stored into its input latch. The sequential programming process is repeated for every desired driver cell. Once the programming is complete, the array update signal, EN2B, is pulsed from high to low, and for each driver, the data held in the input latch of the dual latch is loaded into the output latch. The data from the output latch sets the output phase of the high voltage driver correspondingly and the array is simultaneously updated with the new output phase configuration.

In this chapter, components of the PFP IC system will be described in detail. In Chapter 4.2, the transistor-level latches and their configuration as memory elements in the shift register and the driver memory will be described. In Chapter 4.3, the high voltage digital driver cell's operation, enable logic, memory storage, and high voltage output transistor will be explained and the array layout of these cells is described in Chapter 4.4. Then, the communications shift register and array address decoders will be described in Chapter 4.5 and Chapter 4.6, respectively. Following that, the design process of the data buffers used to buffer the signals with large fan-out will be described in Chapter 4.7. Finally, the circuitry and components designed to facilitate DEP assisted droplet injection will be discussed in Chapter 4.8.

4.2. Memory Elements Used in the PFP IC Electronics

4.2.1. D Latch

The building block of the memory storage elements used in the PFP IC is a 1-bit latch called D Latch (DL) and its transistor-level schematic is shown in Figure 4-2. The latch has three inputs: the data input D, the active-low enable signal CLKB, and the active-low reset signal CLRB; and two outputs: Q and /Q.

The four PMOS transistors (MP2, MP3, MP8, MP9), four NMOS transistors (MN2, MN3, MN8, MN9) and a two-input NOR feedback gate produces the latching behavior of the circuit. The D input signal is connected directly to the gates of MP2 and MN2, while the input signal CLKB is passed through an inverter, generating its complement for the gates of MN8 and MP9 and through another inverter, generating the inputs to MP8 and MN9. The reset signal CLRB is complemented by an inverter and brought to the NOR gate for implementation of the reset function. The output of the NOR gate NOROUT is the logical latch output, but is buffered by output inverters. One inverter buffers NOROUT to generate the output complement /Q, while two separate inverters buffer NOROUT to produce Q.

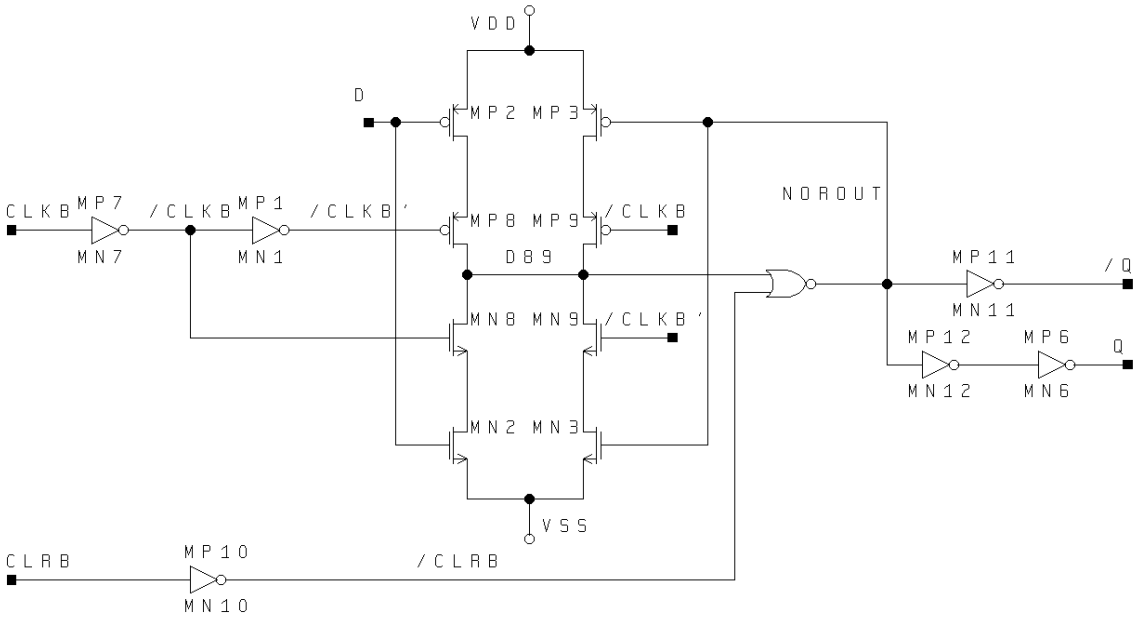


Figure 4-2 Transistor and gate-level schematic of the DL

Table 4-2 Truth table for the DL

CLKB	D	Q^+	$/Q^+$
0	0	0	1
0	1	1	0
1	0	Q	/Q
1	1	Q	/Q

The input-output relationship of the latch when the reset signal CLRB is not enabled is shown in Table 4-2. According to the truth table, when the CLKB signal is high, the latch holds the stored data at the output Q. When the CLKB signal is low, the latch sets the output Q to the input data D.

The reset capability of the latch is facilitated by the two-input NOR gate, which also produces the output of the latch. The inputs to the two-input NOR gate are /CLRB, the reset signal's complement, and D89, the logic at the drains of MN8, MN9, MP8, and MP9. The transistor-level schematic of the two-input NOR gate is shown in Figure 4-3

and its truth table is shown in Table 4-3. When the latch input CLRB is logic low, its complement, /CLRB, is logic high and the output of the two-input NOR gate, NOROUT, is logic low regardless of the signal D89. This resets the Q output to logic low and /Q to logic high. However, when the latch input CLRB is logic high, its complement, /CLRB, is logic low and NOROUT is determined by D89. The signal D89 sets NOROUT and thus the output Q to its complement. Therefore, when CLRB is high, the two-input NOR gate behaves like an inverter and the latch operates normally.

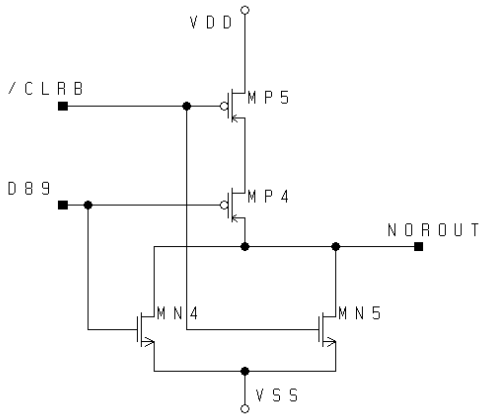


Figure 4-3 Two-input NOR gate used in D latch

Table 4-3 Truth table for the two-input NOR gate

/CLRB	D89	NOROUT
0	0	1
0	1	0
1	0	0
1	1	0

To understand the operation of the latch a simplified version of the circuit is analyzed. In the simplified latch, it is assumed that CLRB is high and that the two-input NOR gate behaves like an inverter as explained earlier. Therefore, the CLRB signal is removed

from the schematic and the NOR gate is replaced with an inverter. The input and output inverter buffers are also ignored in this analysis. In addition, NOROUT has been renamed OUT since it gives the same logical output as Q, the node name /CLKB' has been reduced to CLKB, and the output connections have been redrawn for clarity. The resulting latch circuit is shown in Figure 4-4.

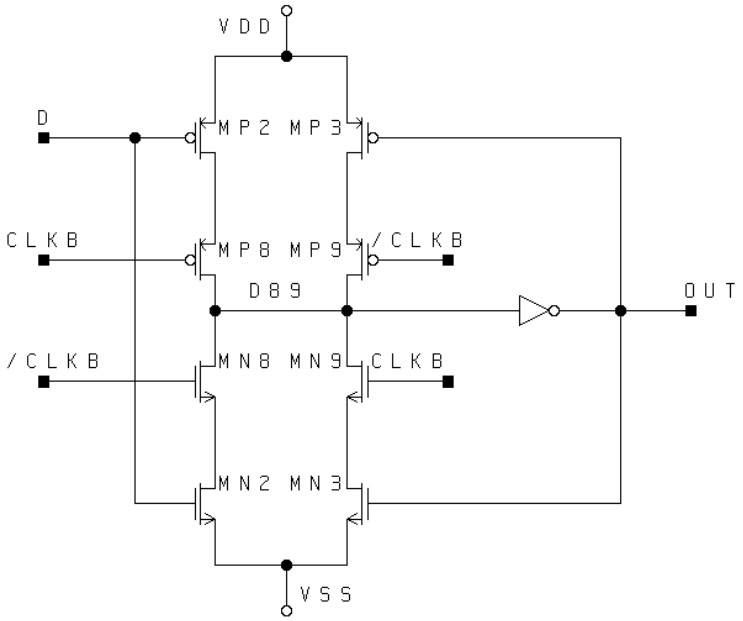
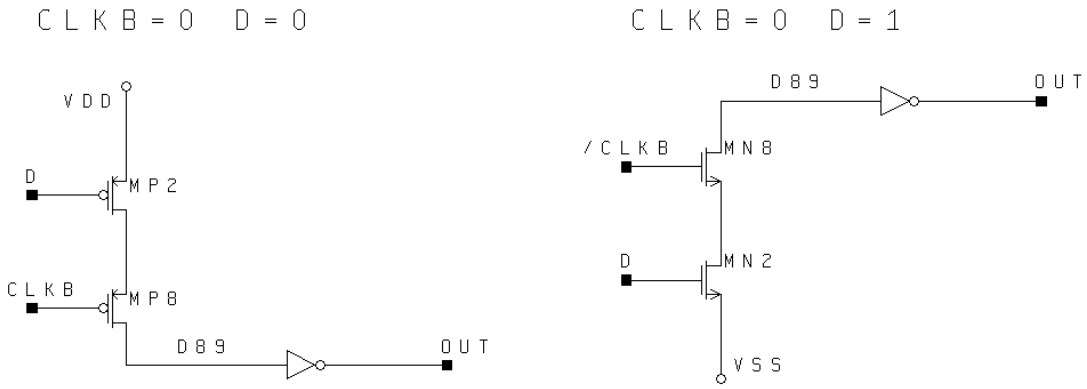


Figure 4-4 Transistor-level schematic of the simplified DL

There are four input combinations for the D and CLKB signals, each of which will be explained next. When CLKB and D are both logic low, the latch is enabled and the output follows the logic low D input. The equivalent circuit for this state is shown in Figure 4-5a. Since D and CLKB are logic low, transistors MP2 and MP8 are on, driving D89 to VDD. The logic high level on D89 is inverted to produce a logic low level at OUT. Similarly, when CLKB is logic low and D is logic high, the latch is enabled and the output follows the logic high D input. The equivalent circuit for this state is shown in

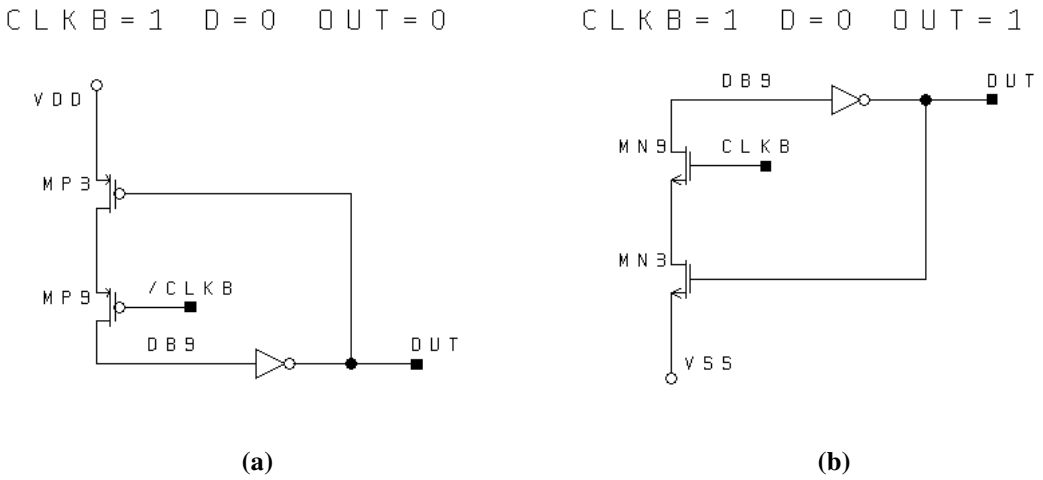
Figure 4-5b. Since CLKB is logic low, /CLKB is logic high, turning on transistor MN8. Also, since D is logic high, transistor MN2 turns on and D89 is driven to VSS. The logic low level at D89 is inverted to produce a logic high level at OUT.



(a) **(b)**

Figure 4-5 Equivalent circuits for the DL when CLRB is high where (a) CLKB is logic low, D is logic low and (b) CLKB is logic low and D is logic high.

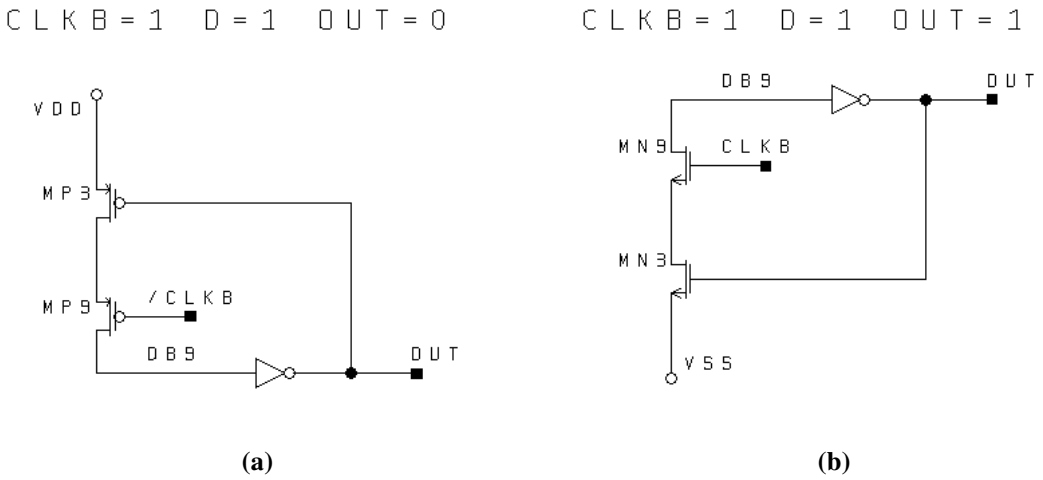
When CLKB is logic high and D is logic low, the latch is in a hold state and OUT is determined by the previous OUT. Since CLKB is logic high and /CLKB is logic low, both MN9 and MP9 are on, respectively. However, the current path driving the D89 is determined by OUT, since OUT feeds back to the gates of transistors MP3 and MN3, determining whether they are on or off. If the OUT was previously logic high, MN3 turns on and D89 is driven to VSS as shown in Figure 4-6a. This holds OUT at a logic high level. Conversely, if OUT was previously logic low, MP3 turns on and D89 is driven to VDD as shown in Figure 4-6b. As a result, OUT is held at logic low.



(a) **(b)**

Figure 4-6 Equivalent circuits for the DL in hold mode when CLRB is logic high, CLKB is logic high, D is logic low where (a) OUT is held at logic low and (b) OUT is held at logic high.

When both CLKB and D are logic high, the DL still operates in the hold mode since D does not change the current path from the power supplies to D89. The operation in this mode is identical to the previous case with D at logic low as shown by the simplified circuits in Figure 4-7a and 4-7b. Both MN9 and MP9 are on since CLKB is logic high and /CLKB is logic low, but the voltage at D89 is determined by OUT, which controls transistors MP3 and MN3. If the previous OUT is logic low, then MP3 is turned on, MN3 is turned off, and the current path from VDD drives D89 to logic high and OUT is driven to logic low. However, if the previous OUT is logic high, then MP3 is turned off, MN3 is turned on, and the current path from VSS drives D89 to logic low and OUT is held to logic high.



(a) **(b)**

Figure 4-7 Equivalent circuits for the DL in hold mode when CLRB is logic high, CLKB is logic low and D is logic high where (a) OUT is held at logic low and (b) OUT is held at logic high.

The operation of the DL with the four input combinations of CLKB and D has been explained and the truth table in Table 4-2 is derived. One thing to notice is that the DL is level sensitive, meaning that the data can change any time while CLKB is logic low. Only after CLKB goes high, does the DL stop feeding the input through to the output and latch the last received logic data.

4.2.2. Dual Latch Configuration

The single D latch that was previously described serves as the basic unit for the dual latch memory used in PFP. The dual latch configuration for the D latch is simply two D latches cascaded together such that the output of the first latch is connected to the data input of the second latch. The dual latch configuration with independent clocks is shown in Figure 4-8. The data input to the memory cell is connected to the D input of the first latch and the output of the dual latch is taken at the output of the second latch. The two have separate clock enable lines, CLKB_A and CLKB_B, but share the same reset signal CLRB.

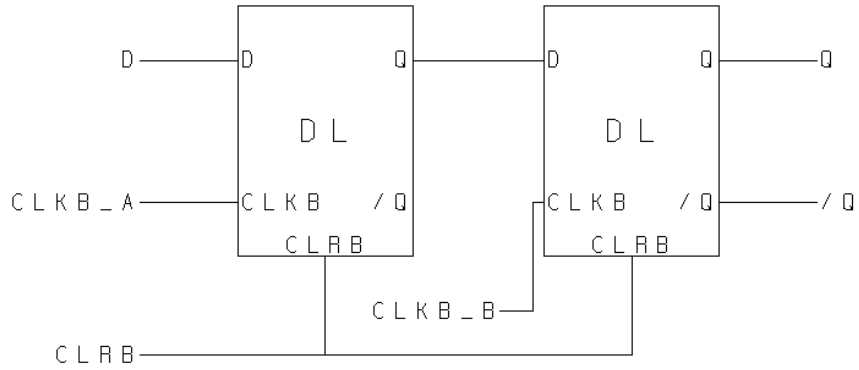


Figure 4-8 Independent clocking scheme for dual latch

In PFP, the dual latch is used with two different clocking schemes. In one configuration, the dual latch is clocked with two signals to enable the dual latches independently. By doing so, the first latch can store new incoming data by enabling CLKB_A, and, when the time is appropriate, the second latch can update the memory output with the stored data by enabling CLKB_B. This clocking scheme allows the dual latch to act as a two-stage latch allowing the first latch to be programmed with new data while the second latch holds the old data until the time is right for the output to be updated with the new data. This method is used in the PFP IC for sequentially programming driver cell memories with new data and then updating them simultaneously.

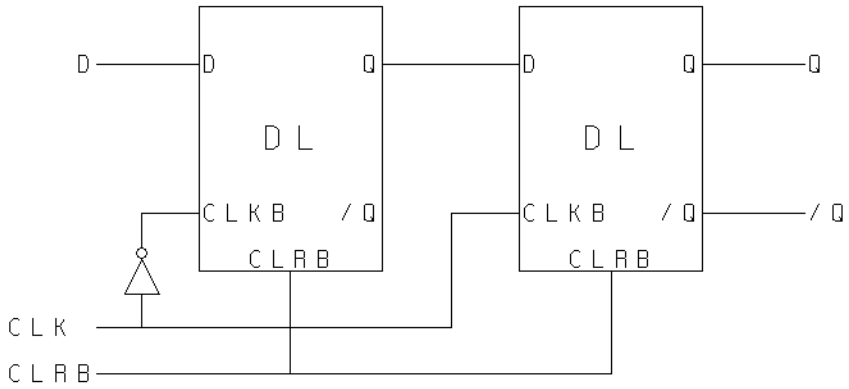


Figure 4-9 Master-slave clocking scheme for dual latch

Another clocking technique used on the dual latch is a master-slave scheme. The master-slave configuration of the dual latch in the PFP IC is shown in Figure 4-9. In this clocking configuration, the first latch receives the complement of the clock signal /CLK while the second latch receives the actual clock signal CLK. When the CLK signal is logic high and /CLK is logic low, the first latch stores the data bit D since it is active-low. Once CLK changes to logic low, the second latch is enabled, the first latch is no longer enabled, and data stored by the first latch is passed to the second latch. These master-slave dual latches are implemented in the shift register. The master-slave clocking scheme allows the level sensitive latch to be configured in a way that eliminates the possibility of a race-condition.

4.3. High Voltage Electrode Driver Cell

The driver cell is composed of three main parts: the high voltage driver, the dual latch memory, and the memory enable logic. In this section, the high voltage driver will be described first, followed by the memory and enable logic.

4.3.1. High Voltage Electrode Driver

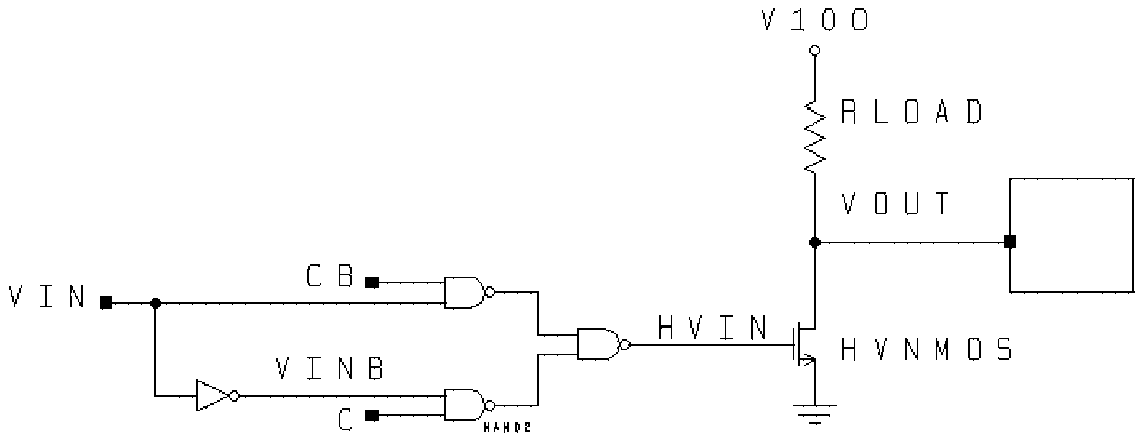


Figure 4-10 Schematic of high voltage digital electrode driver

Description of the digital driver

The high voltage digital driver used in the electrode array cell is shown in Figure 4-10. It consists of a high voltage NMOS transistor configured as a resistively loaded high voltage pull down transistor and a NAND gate multiplexer that allows control over the phase state of the output signal, VOUT. Three input signals control the operation of the digital driver. The input VIN serves as the reference for the phase state of the digital driver output. Normally, VIN is a 5V square wave, which translates into a square wave at VOUT with a peak to peak amplitude set to V100. The control signal C and its complement CB set the phase of the output signal relative to the input reference square wave.

Operation of the high voltage electrode driver

The electrode is connected to the drain of the high voltage transistor at node VOUT. The signal at VOUT is determined by the high voltage transistor's on and off state, which is controlled by its gate voltage HVIN. When HVIN is low, the transistor is turned off and

the output VOUT is pulled to V100 through the resistive path. When HVIN is high, the transistor is turned on and pulls the output node voltage down to a voltage near ground. Periodically switching the gate of the high voltage transistor on and off will produce a square wave output at VOUT. Since the desired output swing is 100V, the output current will be 20uA through the 5Mohm RLOAD when the high-voltage transistor is turned on and pulling VOUT to a low voltage near ground.

Depending on the control signal C and its complement CB, the two-input NAND gate multiplexer passes either the external square-wave signal VIN or its complement VINB to HVIN. The signals C and CB determine whether the output is 0 or 180 degrees in-phase with the input signal VIN. When C is logic high and CB is logic low, VINB sets the voltage at HVIN and the output is 0 degrees in-phase with the input VIN. However, when C is logic low and CB is logic high, VIN sets HVIN and the output is 180 degrees in-phase with the input VIN. The multiplexer is implemented using three 2-input NAND gates executing the logic function

$$HVIN = (CB \bullet VIN) + (C \bullet VINB).$$

The VINB signal is generated from VIN through the inverter and the C and CB logic levels are determined by the output of the driver cell's dual latch memory. The truth table and state designation for the high voltage digital driver circuit is shown in Table 4-4.

Table 4-4 Truth table for the high voltage digital driver circuit

C	CB	VIN	VINB	HVIN	VOUT	Phase State
0	1	0	1	0	1	Out-of-Phase
0	1	1	0	1	0	
1	0	0	1	1	0	In-Phase
1	0	1	0	0	1	

As explained in Chapter 3, the digital driver uses an NMOS with resistor load rather than a CMOS output driver circuit due to the limited breakdown of CMOS circuits in this SOI process. One disadvantage of the NMOS with resistor load is the static power dissipation during the transistor's on state. When the NMOS is turned on, a static current Iout=V100/Rload results. At V100=100V and RLOAD=5Mohm, this results in a static current of Iout=20uA and a static power dissipation of 2mW.

4.3.2. Driver Cell Dual Latch Memory and Memory Enable Logic

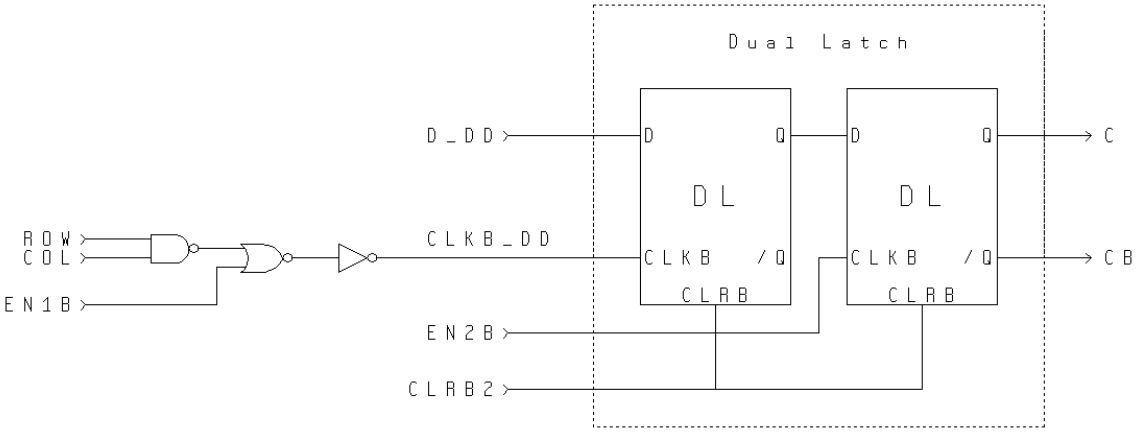


Figure 4-11 Schematic of the driver cell memory connected to the memory enable logic

The driver cell's memory enable logic and dual latch memory are shown in Figure 4-11. The driver cell uses a dual latch with independent enable signals as described in Chapter 4.2.2 to store its phase state data. The signals EN1B and EN2B are the enable signals that control the driver memory. The signal EN1B indirectly enables the data input latch,

while EN2B directly controls the output latch. The Q output of the dual latch is connected to the C input of the high voltage driver and the QB output is connected to the CB input of the high voltage driver. A logic low C causes the digital driver output to be 180-degrees in-phase with the square-wave input, while a logic high C causes the output to be 0-degrees in-phase with the square-wave input.

The memory enable logic allows only the driver cell with the enabled row and column lines to receive the EN1B signal by controlling the passage of EN1B into the driver cell's memory. Only when the row and column lines are logic high can EN1B be passed to the target cell's memory and enable the latching of the new data into the input latch. This ensures that only one driver cell can be programmed at a time. The characteristic equation for the enable logic is

$$CLKB\_DD = \overline{(ROW \bullet COL)} + EN1B$$

The truth table for the digital driver enable logic is shown in Table 4-5. The enable input of the first latch, CLKB_DD, will be logic low only when EN1B is logic low and both ROW and COL are logic high.

Table 4-5 Truth table for Digital Driver enable logic

EN1B	ROW	COL	CLKB_DD
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

The asynchronous active low CLRB2 signal resets the dual latch in the driver cell to logic low.

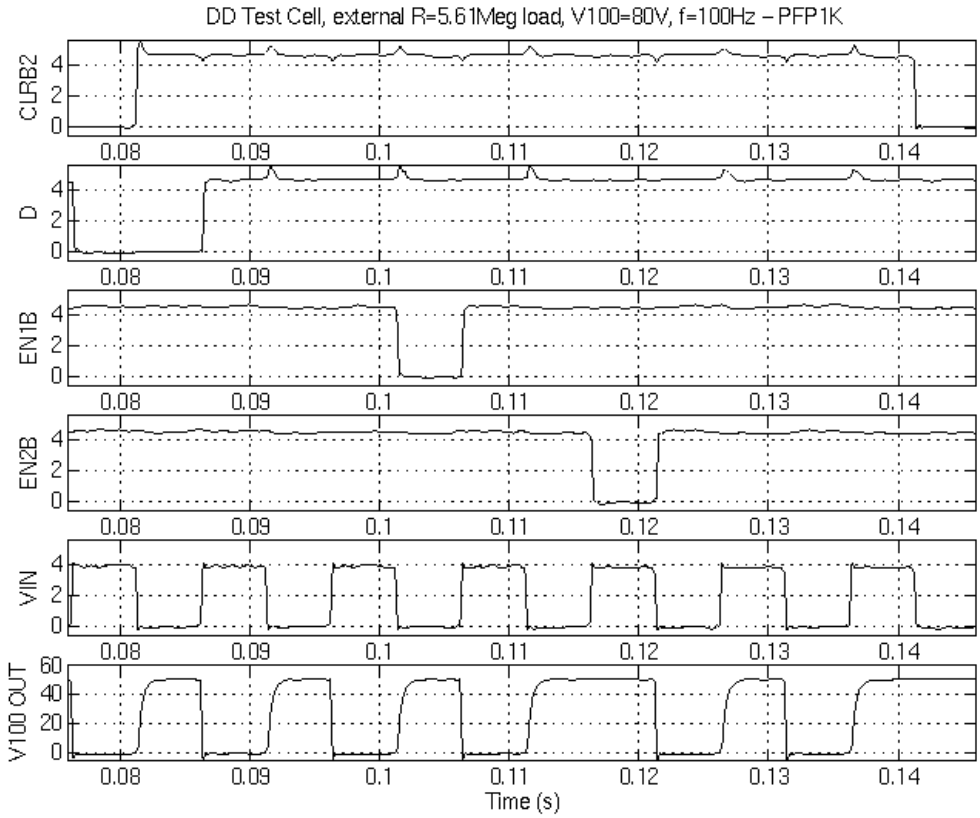


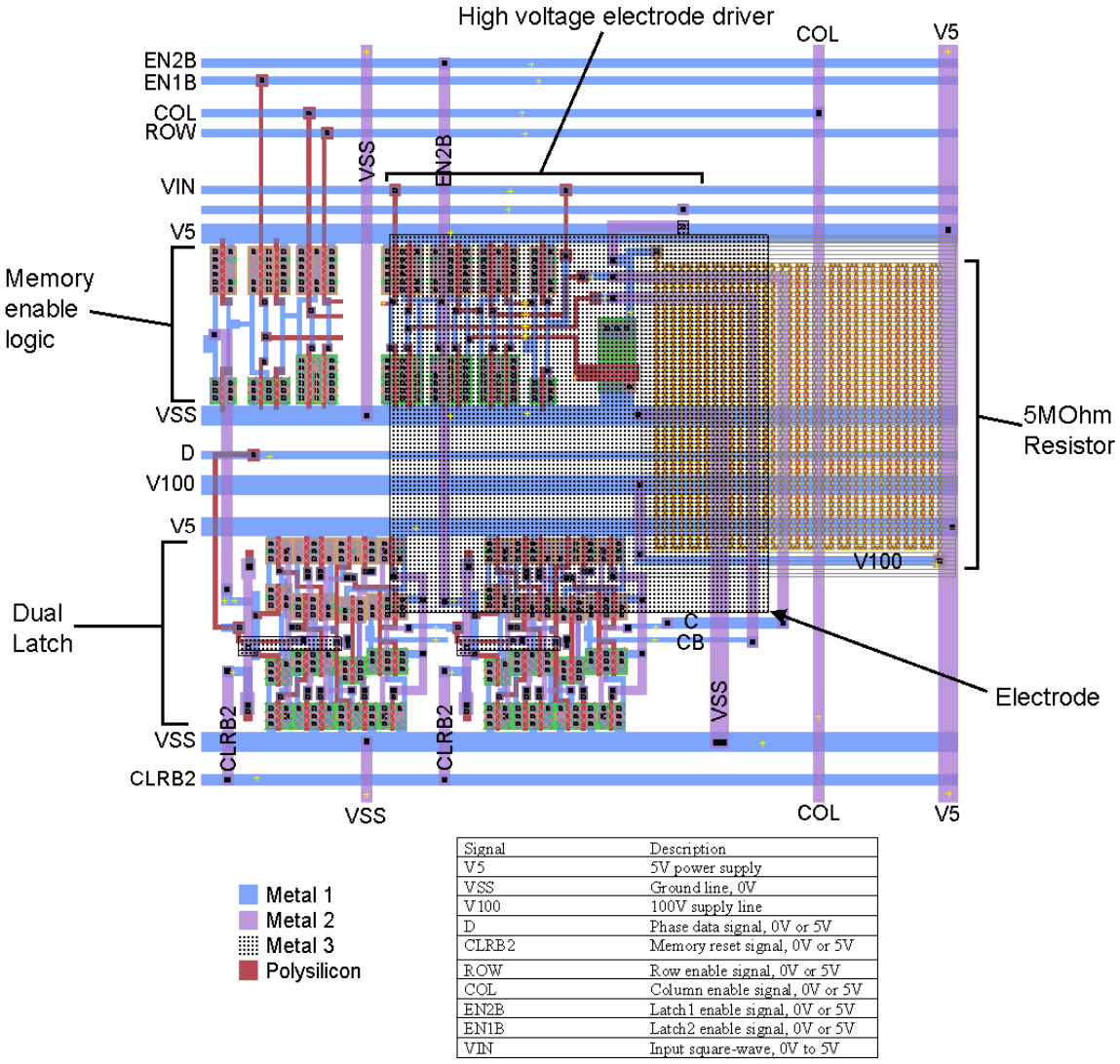
Figure 4-12 Timing diagram of the digital driver test cell from experimentation illustrating its phase change and high voltage output capability

The results of a transient experiment demonstrating the operation of the digital driver test cell on PFP1K is shown in Figure 4-12. According to the figure, at about time t=0.081s, the CLRB2 signal is disabled and at time t=0.086s, a logic high is applied to the D data input. At t=0.101s, the EN1B is set to logic low, latching the input data into the input latch of the digital driver's dual latch memory and then set back to logic high at t=0.106s. At t=0.116s, the EN2B signal is set to logic low, updating the output latch of the dual latch and causing the output, V100_OUT, to change phases and is then set back to logic high at t=0.121s. At t=0.141s, the CLRB2 signal is set to logic low, which resets the

output phase state of V100_OUT. The experiment confirms the programmability and correct phase state operation of the digital driver circuit.

4.3.3. HV Digital Driver Cell and Digital Driver Array Layout

The digital driver cell layout is square such that it can be tiled to form the 32-by-32 cell digital driver array. The dimensions of the layout are 200um by 200um, making the total area of the array alone to be 6400um by 6400um. The layout of an individual digital driver cell is shown in Figure 4-13. The signal lines run horizontally on M1 across the cell, with the exception of the vertical M2 column line and the extra vertical VSS and V5 supply lines. Arranging the routing in this way allows the signal lines to be connected across the span of the array once the cells are tiled together. A description of the signal lines is also given in the table shown in Figure 4-13.



Signal	Description
V5	5V power supply
VSS	Ground line, 0V
V100	100V supply line
D	Phase data signal, 0V or 5V
CLRB2	Memory reset signal, 0V or 5V
ROW	Row enable signal, 0V or 5V
COL	Column enable signal, 0V or 5V
EN2B	Latch1 enable signal, 0V or 5V
EN1B	Latch2 enable signal, 0V or 5V
VIN	Input square-wave, 0V to 5V

Figure 4-13 Layout of the digital driver array cell showing the high voltage electrode driver, memory enable logic, dual latch memory, 5Mohm resistor and electrode and identifying key signal lines.

A subsection of the driver cell array is shown in Figure 4-14, illustrating the interconnect between adjacent cells. The signals are routed out towards the decoders and shift register at the left of the array. The high voltage electrode is a 100um-by-100um layer of M3, the topmost metal layer, and centered within the driver cell. With a cell size of 200um-by-200um, the electrodes are spaced 100um from each other.

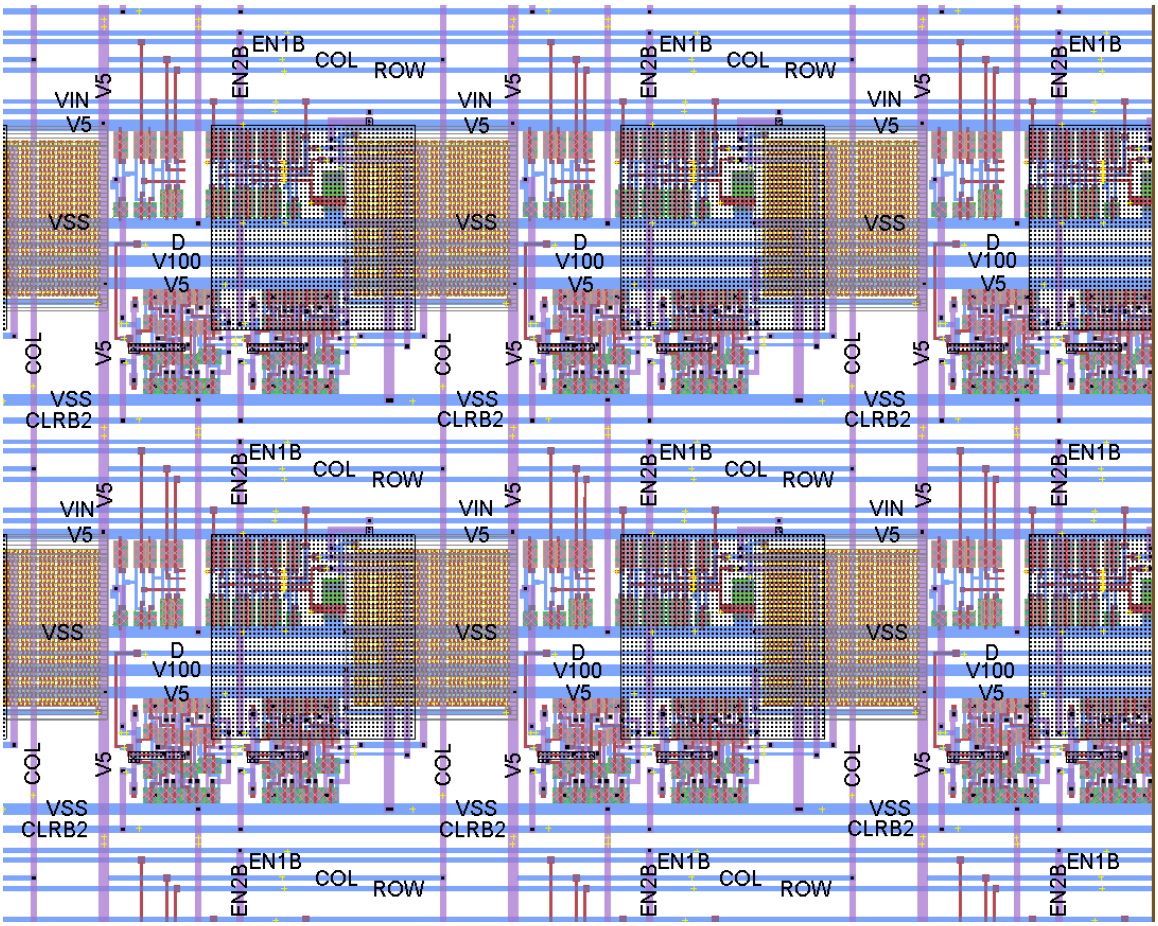


Figure 4-14 Subsection of the digital driver array showing 4-by-4 digital driver cells connected together in a tiled fashion with routing spanning across the cells

4.4. 11-bit Communications Shift Register

Description of the shift register

The shift register communicates data from the external serial data input DATA_IN to the PFP IC system and is shown in Figure 4-15. The shift register is composed of 11 dual latches operating in a master-slave configuration. The 11 dual latches are can be divided into three sections. The first memory element at the top of the shift register stores the new phase state data bit for the targeted cell. The following five memory elements store the 5-bit row address of the target cell and the last five memory elements store the 5-bit

column address of the target cell. Each memory of the shift register uses the master-slave dual latch configuration described in Chapter 4.2.2.

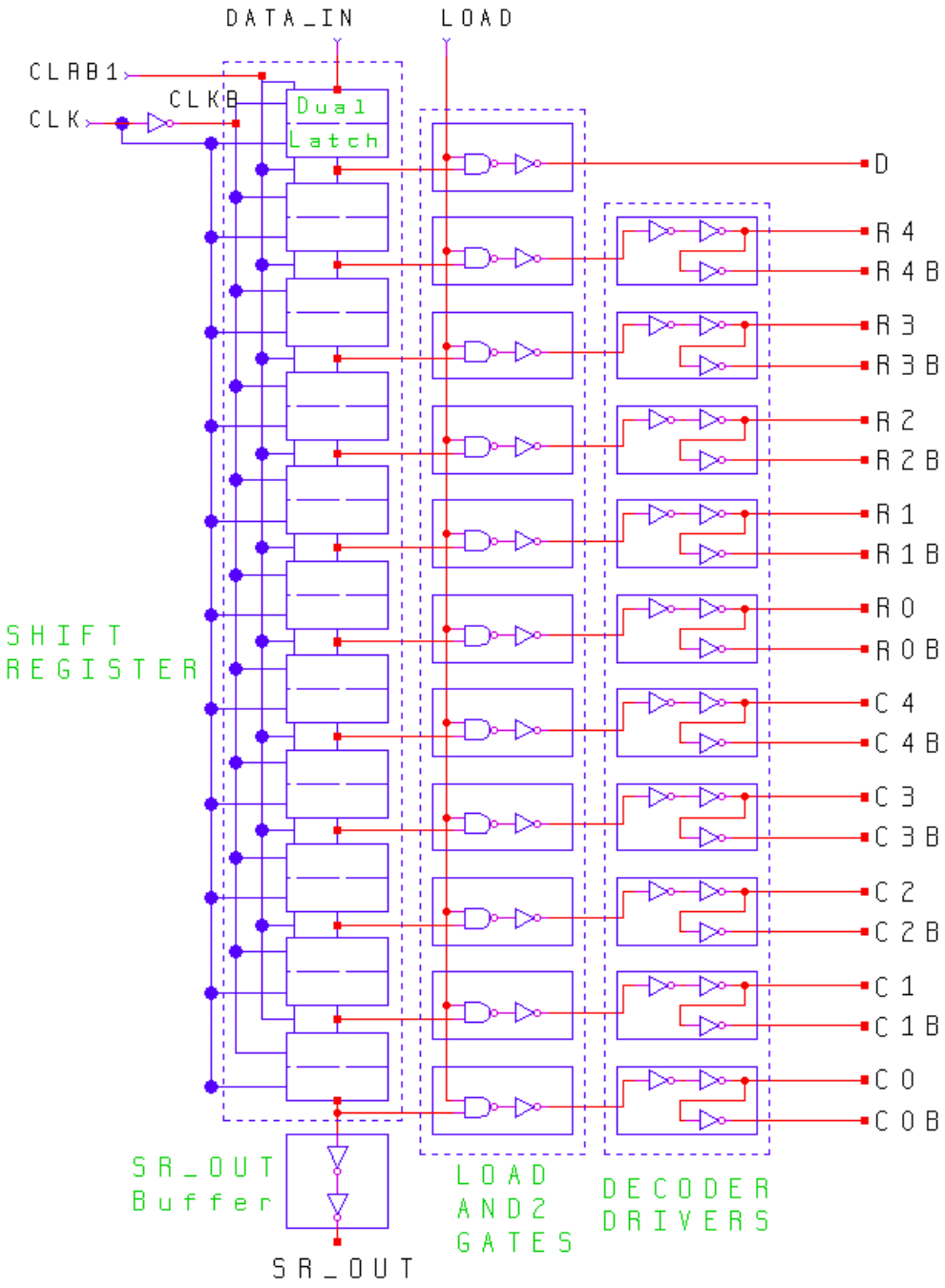


Figure 4-15 Schematic of 11-bit communications shift register with 11 2-input AND gates controlling the parallel outputs of the shift register and decoder driving buffers

Operation of the shift register

The shift register has one serial data input DATA_IN, eleven parallel data outputs and one serial data output SR_OUT for testing purposes. The parallel outputs are propagated to the rest of the system through 2-input AND (AND2) gates controlled by the LOAD signal. The AND2 gates shown in Figure 4-15 prevent data from the shift register to reach the other parts of the system while the shift register is still loading the data sequence. The loading of data into the master-slave dual latches is controlled by the clock signal CLK and its complement CLKB. When CLK is logic high, the input latch of every dual latch is enabled. When CLK is low, the output latch of every dual latch is enabled. Thus, when the CLK transitions from H→L, each dual latch passes its data to the following dual latch in the shift register and the first dual latch receives data from the DATA_IN input. In order for data to be latched properly by a memory element, the data must be stable during the H→L transition of the CLK. The shift register is asynchronously reset to logic low by the active low CLRB1 signal.

During a programming cycle, the address and state data are loaded into the shift register. Once the shift register contains the data sequence, the data is passed to the other parts of the PFP IC system by activating the LOAD signal. The row and column addresses are sent to their respective decoders, which enable the row and column lines that correspond to the target cell location. The new phase state data (D data bit) is passed to every standard driver cell in the array through signal buffers (D buffers). The D buffers and the address buffers are discussed in detail in Chapter 4.6.

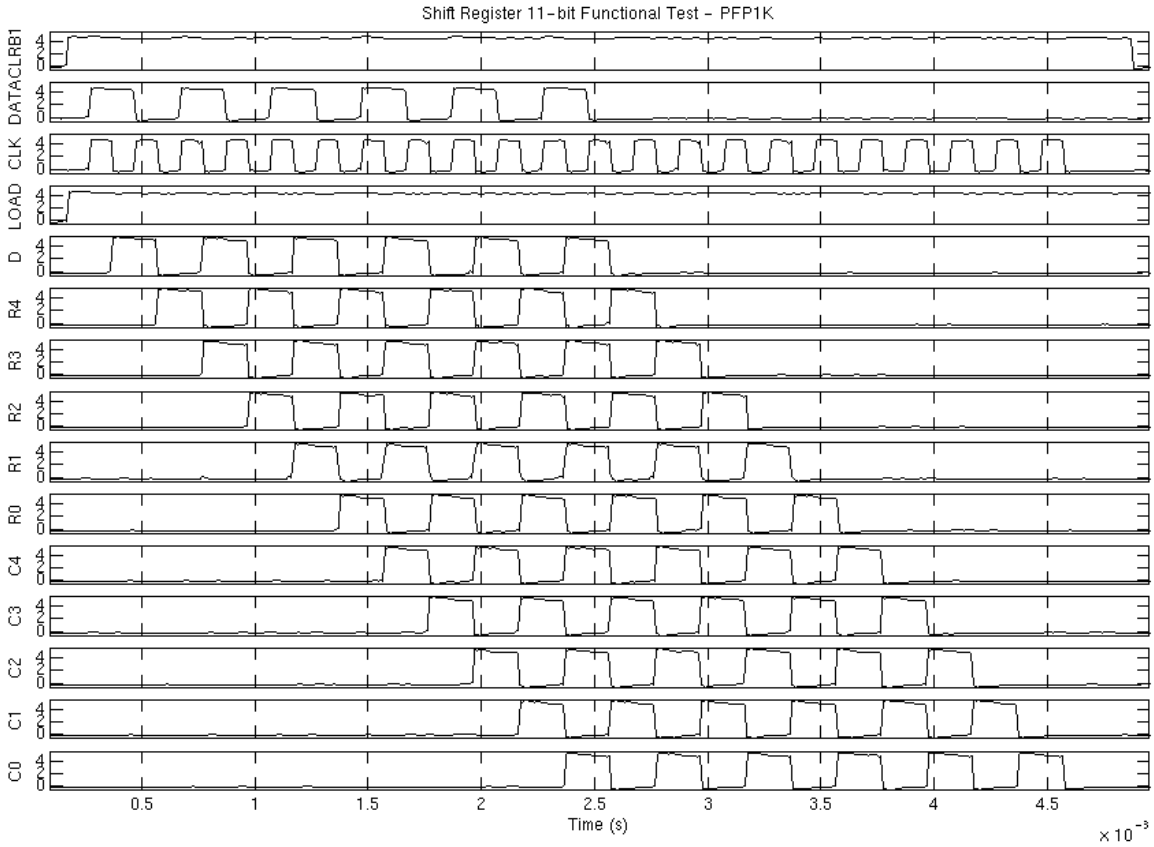


Figure 4-16 Timing diagram of the shift register functional verification showing correct propagation of an alternating sequence of bits

A transient experiment showing the operation of the shift register is shown in Figure 4-16. A series of alternating high and low logic bits is passed into the shift register DATA input with a 5kHz CLK signal. The parallel outputs of the shift register are monitored. The logic sequence at each shift register output is the same as the DATA input sequence delayed by their respective position within the shift register. The timing diagram verifies the correct operation of the shift register.

4.5. 5-bit Address Decoder

Description of the decoder

The 5-bit address decoder decodes the row or column address provided by the shift register by translating the address and enabling the corresponding row or column line of the digital driver array. Each has ten inputs for the 5-bit address and address complement and 32 output lines, one for each enable line. This type of 5-bit decoder is used for both row and column addresses. Figure 4-17 shows the decoder connected to the row address and driving the ROW lines for illustration.

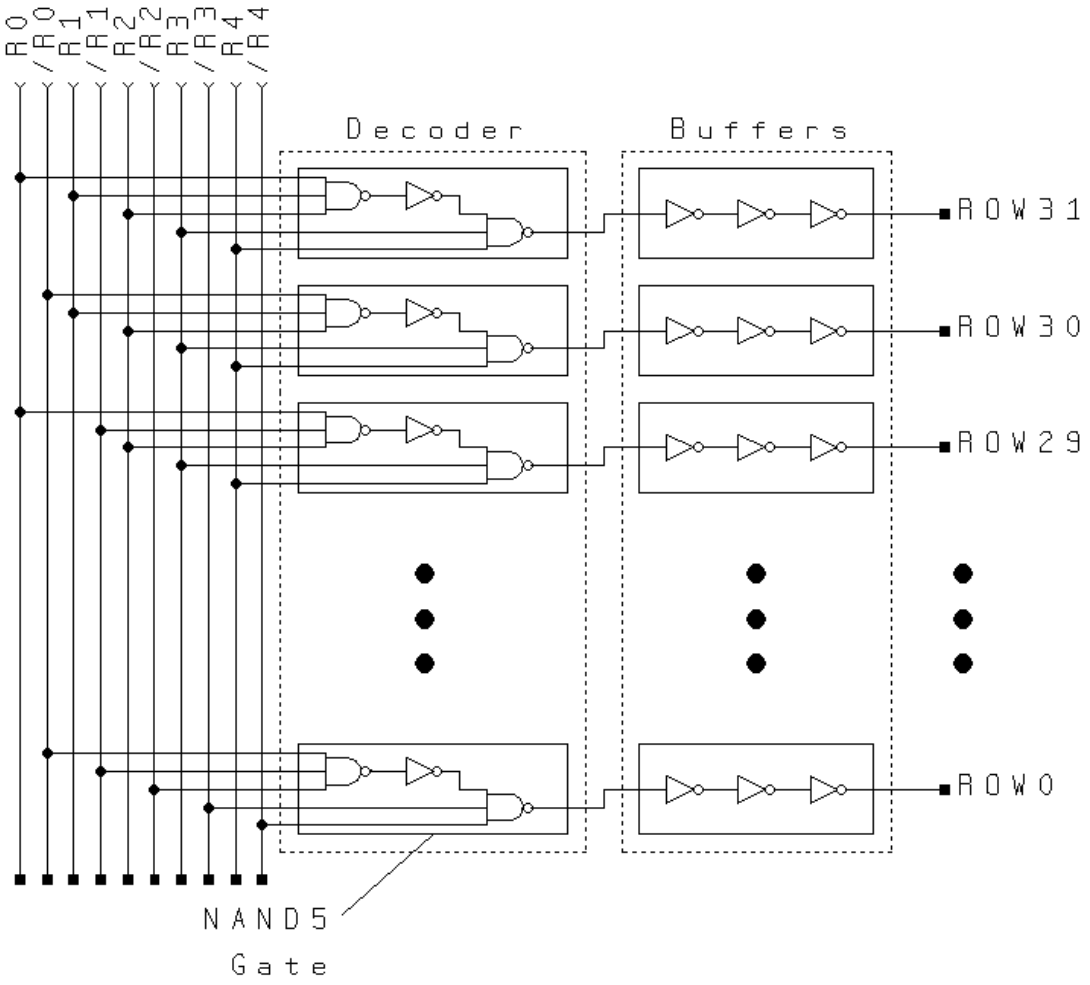


Figure 4-17 Gate-level schematic of the 5-Bit Decoder configured for the ROW address

The decoder is composed of 32 individual decoder cells, one for each permutation of the 5-bit address and configured to drive one array enable line. The decoder cell is composed of a 5-input NAND gate combined with a three-inverter buffer to realize a 5-input AND gate that enables its designated output line if the address bits at its inputs are satisfied. The output buffer is used since each decoder cell must drive a large fan-out of 32 logic gates. The decoder output buffer is described in detail in Chapter 4.7.

Operation of the Decoder

The operation of the row decoder used in PFP1K is shown in Figure 4-18. In the test, five available ROW monitor lines are used to test the output of the decoder: ROW15, ROW14, ROW13, ROW12, and ROW11. The shift register is loaded with a binary data sequence composing the addresses 15, 14, 13, 12 and 11 in sequence. As the data sequence is clocked into the shift register, the 5-bit row address will eventually be available in the row address memory section of the shift register. When this occurs, the LOAD signal is activated and the row data are sent to the row decoder. The row decoder then enables the corresponding line and the ROW line pulse is high for as long as the LOAD signal is active. The signals on those available row lines are monitored to verify correct operation.

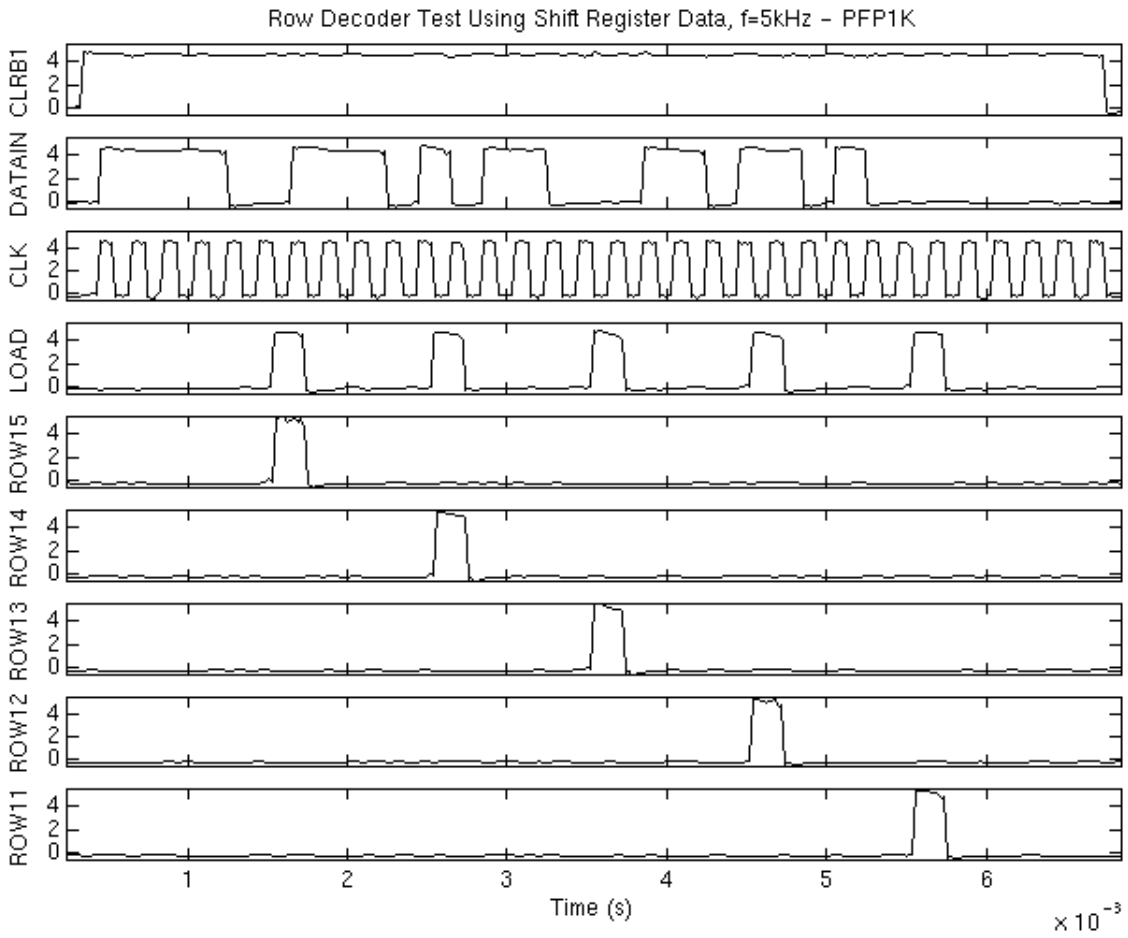


Figure 4-18 Timing diagram of the 5-bit row decoder functional verification experiment by loading 5 different row addresses into the decoders through the shift register and monitoring the corresponding row enable lines

The column decoder is tested in the same way as the row decoder and the timing diagrams are shown in Figure 4-19. However, the available decoder output monitor lines are COL20, COL19, COL18, COL17 and COL16. The data corresponding to this sequence of column addresses are sent into the shift register. At the appropriate time when the desired column address is present at the column decoder address portion of the shift register, the LOAD signal is activated, sending the column address to the column decoder. The column decoder then decodes the address and enables the corresponding

column enable line. This is done for all five of the available column monitor outputs. The experiment verifies the correct operation of the column decoder and its output buffer.

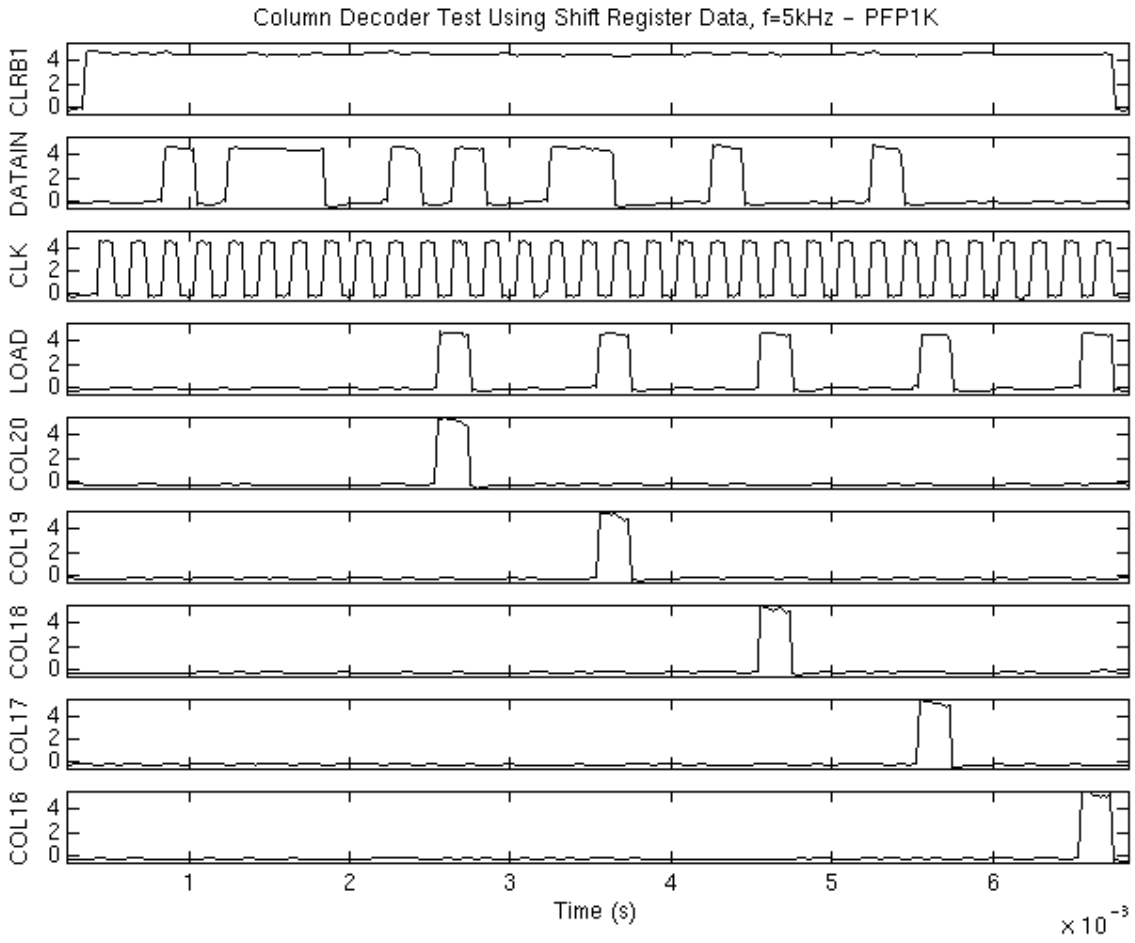


Figure 4-19 Timing diagram of the 5-bit column decoder functional verification experiment by loading 5 different column addresses into the decoders through the shift register and monitoring the corresponding column enable lines

4.6. Design of Buffers for Signal Lines with Large Fan-out

4.6.1. Introduction to the Buffer Design

One of the major concerns with the full sized PFP IC system is the large loading of internal signal lines on the PFP IC component outputs. Some of the signals that need to drive multiple logic gates are the D data from the shift register to the array, the ROW and

COL enable lines from the decoder to the array and the address data from the shift register to the decoders. For example, each address bit from the shift register AND2 output gate output must drive 16 logic gates at the decoder inputs and each ROW or COL line from the decoder output must drive 32 logic gates at the enable logic inputs from the digital driver array cells. The concern is that this loading will affect the speed of the circuit and overall performance by increasing rise, fall and propagation delay times.

The issue of loading is more prominent in PFP1K because of the larger array and larger decoders. PFP3 has a much smaller array in comparison and therefore smaller decoders. To compare, the PFP3 system has 2-bit addresses for the row and column, each driving only 4 gates each on the driver array, while the PFP1K has 5-bit addresses for the row and column, each driving 32 logic gates as stated earlier. Therefore, the loading can be seen as a much larger problem as the array becomes larger in the PFP1K chip.

To address the problem of large fan-out, buffers composed of inverters are designed to drive the heavily loaded signals on the PFP1K system. The number of inverters per buffer is arbitrarily chosen to allow for gradually larger inverters, while the widths of the transistors used in the inverters are optimized using the optimization procedures in HSPICE. In this section, the signals that drive large loads will first be identified. Then, the buffer placement, design specifications and optimization procedure will be explained. Finally, the layout of the inverter buffers and their placement within the circuitry will be discussed.

4.6.2. Problem Areas

There are three major signal path areas of concern. They are the D data line from the shift register AND2 output gates to the driver array, the ROW and COL enable lines from the decoders to the driver array and the two 5-bit addresses from the shift register output AND2 gates to the decoders. The D data from the shift register output AND2 gates must be able to drive the input latch of the dual latch memory of every digital driver cell, resulting in a fan-out of 1024 logic gates. Every row and column enable line must drive 32 logic gates at the digital driver enable logic of an entire row or column line, respectively. Each address data bit from the shift register output AND2 gates and each of its complements must drive 16 logic gates at the decoder inputs.

4.6.3. Timing Specifications for Optimizations

The goal of the buffer design is to reduce the propagation delay of the signals and to ensure that the data are stable by the time the external control signals are activated. The signal paths of the D data and the address data are asymmetric and so the time it takes these signals to arrive at the driver array is also asymmetric. Design choices must be made regarding the timing specifications and the points along the data path for which this performance specification is measured.

The design of the buffers initially involved only the D data line from the shift register output AND2 gates to the driver array and the ROW/COL enable lines from the decoder to the driver array as these are the only internal signals driven by on-chip components that are loaded by the driver array. However, since the shift register address outputs are

also significantly loaded by the decoder, buffers between the shift register outputs and the decoder inputs were also designed. The D data buffer specifications will be presented first, followed by the ROW/COL enable buffer specifications. Thirdly, the address data buffer specifications will be discussed.

4.6.3.1.D Data Buffer Specifications

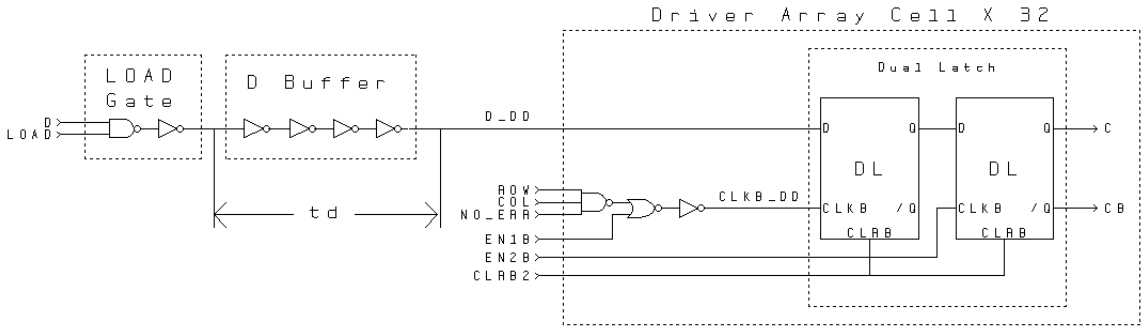


Figure 4-20 Propagation path for the D data signal from the shift register output AND2 gate to the digital driver memory

The propagation path for the D data signal from the shift register to the digital driver cell is shown in Figure 4-20. The buffer is composed of four inverters of different sizes and is placed between the shift register output AND2 gate and the digital driver. When the LOAD signal is activated, the stable D data bit is sent through the buffer to the driver cells it is loading. Designing for a single buffer capable of driving all 1024 cells of the driver array is not practical due to the potential size of that single buffer. Instead, the task of driving the D signal to the array is broken up by placing a buffer capable of driving 32 cells at each row of the array. Figure 4-20 only shows only one driver cell connected to the output of the buffer, but 32 are used in the optimization and that is noted in the figure. Since the D buffers are broken down into this way, an additional buffer was inserted to drive the inputs of these 32 D buffers. A D buffer like the ones loading the array is used

for this extra D buffer which is situated at the output of the shift register output AND2 gate to drive the inputs of the D buffer at every row of the driver array.

In the optimization routine, D is set to logic high while the LOAD signal is set to a pulse transitioning from L→H and then H→L. The pulse allows the D signal to propagate through the path and to the driver cells, mimicking the data flow during an actual PFP IC programming cycle. Three measurements are used as the criteria for optimization. They are the 50% to 50% propagation time from the input to the output of the buffer for L→H and H→L transitions; the 10%-to-90% rise time and 90%-to-10% fall time of the D data at node D_DD.

4.6.3.2.ROW/COL Enable Buffer Specifications

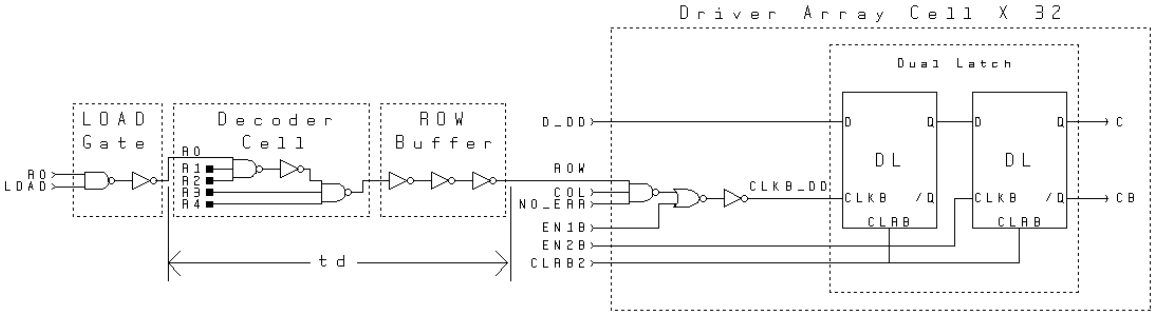


Figure 4-21 Propagation path for the ROW/COL enable signal from the shift register output AND2 gate to the digital driver enable logic

The propagation path for the ROW signal is shown in Figure 4-21. The path is the same for the COL signal, but the ROW signal is used here for illustration. The ROW/COL buffer is located between the output of the decoder and the input of the driver cell's enable logic. The buffer is composed of three inverters, correctly inverting the output of the NAND-implemented decoder cell. When the LOAD signal is activated, the address

bits from the shift register are sent to the decoder and the corresponding ROW is enabled. Only one digital driver cell is shown in Figure 4-21, but each ROW/COL buffer loads the enable logic of 32 driver cells.

A pulse is used for the LOAD signal with R0 at logic high to measure the timing specifications. The optimization routine optimizes based on the 50%-to-50% H→L and L→H delay times from the input of the decoder to the output of the ROW/COL buffer; the 10%-to-90% rise and 90%-to-10% fall time of the ROW signal at the node ROW shown in Figure 4-21.

A design choice is made here regarding the measurement location. The timing measurement can be taken from the LOAD gate output to the CLKB_DD input of the dual latch. If this is done, the signal's arrival time can be synchronized with the propagation time of the D data and thus eliminate any race condition to the latch. However, the actual circuit will not allow the ROW or COL line to propagate directly to the latch. Instead, it waits until the EN1B signal is set before the ROW and COL data can be passed to the latch. Since allowing variation in the timing of the EN1B signal relative to the LOAD signal is desirable, it cannot be assumed that EN1B will be set before the ROW or COL data reaches the respective NOR gate. Thus, to simplify the matter, the measurement is taken to the output of the buffer, only accounting for the delay contributed by the decoder and the buffer.

4.6.3.3.Address data buffer specifications

The data path of the address buffers is shown in Figure 4-15. The address buffers are placed between the address outputs of the AND2 gates and the decoder inputs. Each buffer is composed of three inverters: the first two produce the address data bit and a third outputs the complement of the address data bit. The complement of the address data bit is generated this way since the decoders require both the address bit and its complement. The address bit complement are stemmed off of a single 3 inverter buffer instead of taken from the shift register's QB output because that would require a total of two AND2 output gates and two two-inverter buffers instead of one AND2 output gate and one three inverter buffer. When LOAD is activated, the address data is passed through the address buffer where the address bit and its complement are sent to the decoders.

The address buffer is optimized based on timing measurements of both buffer outputs. The 50%-to-50% H→L and L→H input to output delay times and the rise and fall times of both buffer outputs are used as the optimization criteria. In the optimization simulation, the LOAD signal is pulsed because this more closely resembles the operation of the PFP IC system during an actual programming cycle. Since the propagation path of the complemented signal is longer due to the additional inverter that it must pass through, its timing specifications are set ideally low in order to reduce the asymmetric propagation of the address bit and its complement.

4.6.4. Buffer Optimization and Implementation

In using HSPICE to optimize the device widths, a decision is first made on how many inverters are used for each buffer. This choice is somewhat arbitrary as long as there are enough stages to allow for needed increases in transistor sizing. Next, the optimization simulation is run with the widths of the designable transistors as parameters.

In the optimization simulation, each inverter is modeled using only one PMOS and one NMOS transistor, minimizing the number of designable parameters for HSPICE to consider. For all optimizations, the initial guess for the transistor width is 25um, the minimum is 13u and the maximum is 300u. The optimization routine will produce large transistor widths that will then be realized over several smaller transistor units. One design constraint in dividing the large transistor into smaller transistors is that the XI10 technology only allows transistors with widths that are multiples of 6um, the width of their standard size transistor cell. Therefore, the transistor widths obtained from the optimizer are rounded to the closest multiple of 6um and then broken up over several transistors based on area usage. After dividing the NMOS and PMOS transistors, the resulting choices of transistor quantity and sizes are simulated and compared with the HSPICE results.

4.6.4.1.D Buffer Results

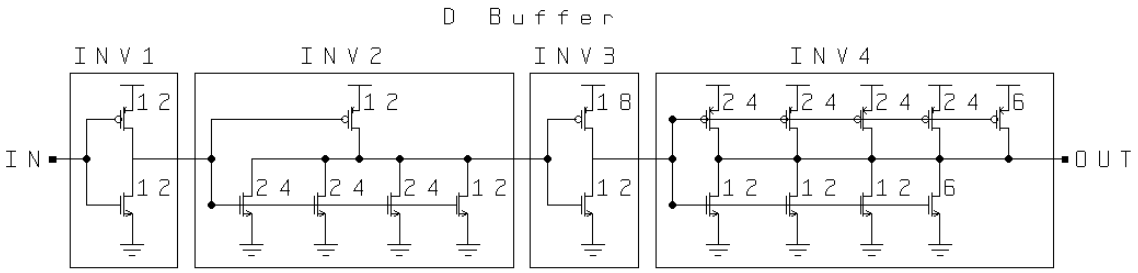


Figure 4-22 Schematic of optimized D data buffer

The schematic of the D buffer is shown in Figure 4-22 and shows the final implementation of the transistor widths. Table 4-6 compares the optimal widths obtained from HSPICE with the implemented transistor widths. Most of the inverters have equivalent widths that are very close to the optimized value.

Table 4-6 D data buffer HSPICE optimized and implemented transistor widths

Transistor	HSPICE Optimal Widths	Implemented Transistor Widths
Inverter 1 PMOS	13.6796um	12um
Inverter 1 NMOS	13.2564um	12um
Inverter 2 PMOS	14.3425um	12um
Inverter 2 NMOS	88.4350um	24um + 24um + 24um + 12um = 84um
Inverter 3 PMOS	15.2063um	18um
Inverter 3 NMOS	13.0000um	12um
Inverter 4 PMOS	107.4424um	24um + 24um + 24um + 24um + 6um = 102um
Inverter 4 NMOS	45.6075um	12um + 12um + 12um + 6um = 42um

The performance measurements of the D buffer are shown in Table 4-7. The table compares the target performance with the optimized performance and the realized performance based on the four optimization parameters: tplh, tphl, tr and tf, which are described in Table 4-7. In general, the optimizer produces widths that achieve the target specifications. The performance of the realized buffers is quite comparable to the optimal buffers and is sufficient in all cases.

Table 4-7 Comparison of the performance of the optimized and the implemented transistor widths of the D buffers by simulation

Parameter name	Parameter Description	Optimization Target (sec)	Optimization Result (sec)	Simulated results based on implemented widths (sec)
t_{pLH}	Output delay L→H	3e-9	2.6558e-9	2.8253e-9
t_{pHL}	Output delay H→L	3e-9	2.9481e-9	2.7665e-9
t_r	Output rise time	1e-9	9.5008e-10	9.9738e-10
t_f	Output fall time	1e-9	1.2068e-9	1.2246e-9

4.6.4.2.ROW / COL Decoder Buffer Results

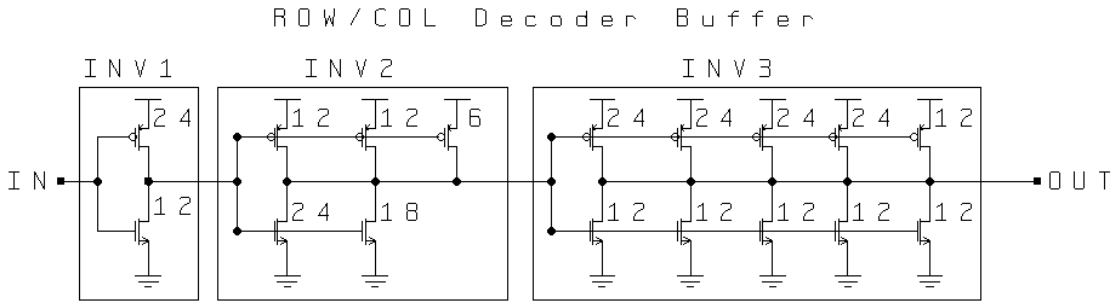


Figure 4-23 Schematic of the optimized row and column decoder output buffer

The transistor-level implementation of the ROW/COL Decoder buffer is shown in Figure 4-23. The schematic shows the transistor widths implemented as multiples of 6um in accordance with the XI10 width requirements. The widths of the optimal transistors are shown in Table 4-8 and compared to the implemented transistor widths.

The ROW/COL buffers are kept the same height as the decoder logic gates to allow easier integration into the decoder cell. Consequently, the widths of the transistors are limited by area, affecting the division of the HSPICE optimized widths into smaller transistors.

Table 4-8 ROW / COL decoder buffer HSPICE optimized and implemented transistor widths

Transistor	HSPICE Optimized Width	Implemented Transistor Widths
Inverter 1 PMOS	22.4474um	24um
Inverter 1 NMOS	13.0000um	12um
Inverter 2 PMOS	33.3430um	12um + 12um + 6um = 30um
Inverter 2 NMOS	41.2126um	24um + 18um = 42um
Inverter 3 PMOS	110.9647um	24um + 24um + 24um + 24um + 12um = 108um
Inverter 3 NMOS	67.6032um	12um + 12um + 12um + 12um + 12um = 60um

The optimizer specification goals of the ROW/COL buffer are shown in Table 4-9 along with the performance times of the buffer using the optimizer widths and the buffer with the implemented widths. The ROW/COL buffer was initially designed to drive 32 digital driver cells. Since the inclusion of the injection circuitry, an additional column of cells has added to the loading resulting in a load of 33 digital driver cells. As an alternative to redesigning the buffer for 33 loads, the original buffer is simulated with 33 digital driver loads and has verified acceptable performance as shown in Table 4-9.

Table 4-9 Comparison of the performance of the optimized and the implemented transistor widths of the ROW / COL decoder buffers by simulation

Parameter name	Parameter Description	Optimization Target (sec)	Optimization Result (sec)	Simulated results based on implemented widths with 32 loads (sec)	Simulated results based on implemented widths with 33 loads (sec)
t_{pLH}	Output delay L→H	3e-9	3.8191e-9	3.7464e-9	4.2177e-9
t_{pHL}	Output delay H→L	3e-9	3.1613e-9	3.3064e-9	3.7939e-9
t_r	Output rise time	1e-9	9.9580e-10	1.0210e-9	2.0991e-9
t_f	Output fall time	1e-9	1.0487e-9	1.1485e-9	2.1283e-9

4.6.4.3.Address Buffer Results

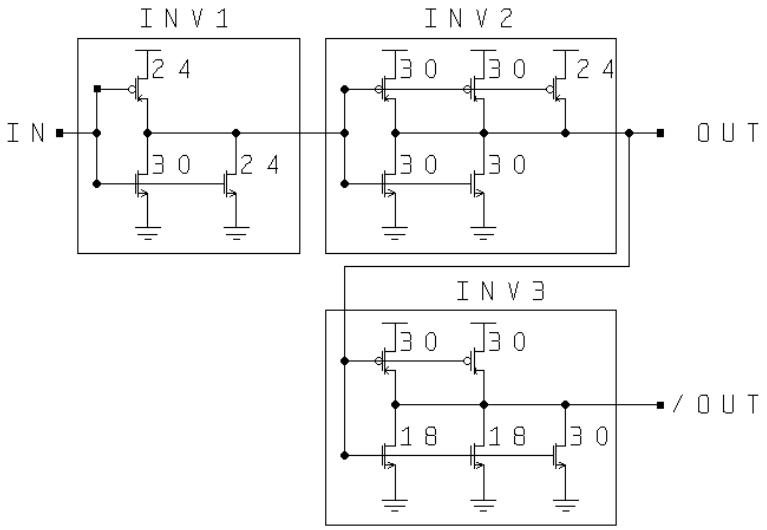


Figure 4-24 Schematic of the optimized address buffer

A transistor-level schematic of the address buffer is shown in Figure 4-24. The buffer is composed of three inverters. The output of the second inverter is the buffered input while the output of the third inverter is the buffered complement of the input. Table 4-10 summarizes the optimization of the address buffers. It shows the HSPICE optimized width parameters and the implemented widths after dividing the optimized width over multiple transistors.

Table 4-10 Address buffer HSPICE optimized and implemented transistor widths

Transistor	HSPICE Optimized Width	Implemented Transistor Widths
Inverter 1 PMOS	22.8675um	24um
Inverter 1 NMOS	52.8557um	30um + 24um = 54um
Inverter 2 PMOS	81.7518um	30um + 30um + 24um = 84um
Inverter 2 NMOS	58.0531um	30um + 30um = 60um
Inverter 3 PMOS	58.6815um	30um + 30um = 60um
Inverter 3 NMOS	69.7738um	18um + 18um + 30um = 66um

The timing goal for the optimization, the performance of the buffers using the optimized widths and the performance of the buffers using the implemented widths are shown in

Table 4-11. Because the ROW/COL buffer is optimized without considering additional buffers between the shift register and the decoder inputs, all the target timing specifications for the address buffer are set to 1ns. The rise and fall time of the output complement is not used in the optimization, but is measured from the buffers using the implemented widths. Although some of the timing results exceed the target specifications, they are still acceptable due to the optimistic goals that were set.

Table 4-11 Comparison of the performance of the optimized and the implemented transistor widths of the address buffers by simulation

Parameter name	Parameter Description	Optimization Target (sec)	Optimization Result (sec)	Simulated results based on implemented widths (sec)
t_{pLH}_1	OUT delay L→H	1e-9	1.0395e-9	1.0192e-9
t_{pHL}_1	OUT delay H→L	1e-9	1.6794e-9	1.6653e-9
t_{pLH}_2	/OUT delay L→H	1e-9	1.6094e-9	1.5559e-9
t_{pHL}_2	/OUT delay H→L	1e-9	2.4149e-9	2.3287e-9
tr_1	OUT rise time	1e-9	1.0069e-9	9.1838e-10
tf_1	OUT fall time	1e-9	8.8819e-10	8.3073e-10
tr_2	/OUT rise time	N/A	N/A	9.1722e-10
tf_2	/OUT fall time	N/A	N/A	5.5705e-10

4.7. DEP Assisted Droplet Injection Circuitry

4.7.1. Requirements for Droplet Injection

As explained in Chapter 2.3.5, in order to facilitate DEP assisted droplet injection, a supplementary force generated by DEP needs to be applied between the injector tip and the collecting electrode. The supplementary DEP force arises from an electric field generated by a potential difference between the injector tip and the collecting electrode. In order to create this potential difference, a common electrode placed under all the injector tips is used to set a reference potential and additional programmable circuitry is used to realize a zero volt ground state at the collecting electrode. By holding this

applied potential difference between the injector electrode and the collecting electrode, droplets of a metered size can theoretically collect and combine to form desired droplets of arbitrary size [1].

4.7.2. Injector Reference Electrode

The reference electrode on the injection side of the chip is shown in the PFP1K chip photograph in Figure 1-2. The reference electrode is composed of all metal, poly and contact layers and is located on the injection side of the chip to the right. A cross sectional view showing the layers of the reference electrode and the distance to the column 31 (COL31) electrodes are shown in Figure 4-25.

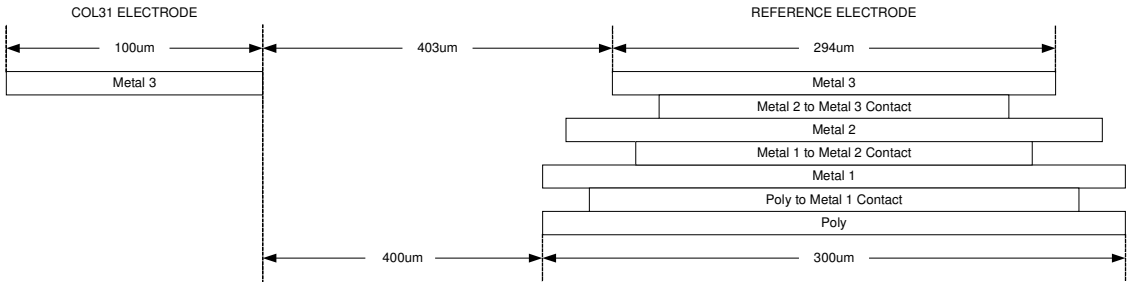


Figure 4-25 Cross sectional view of the injection reference electrode relative to the output electrode of column 31

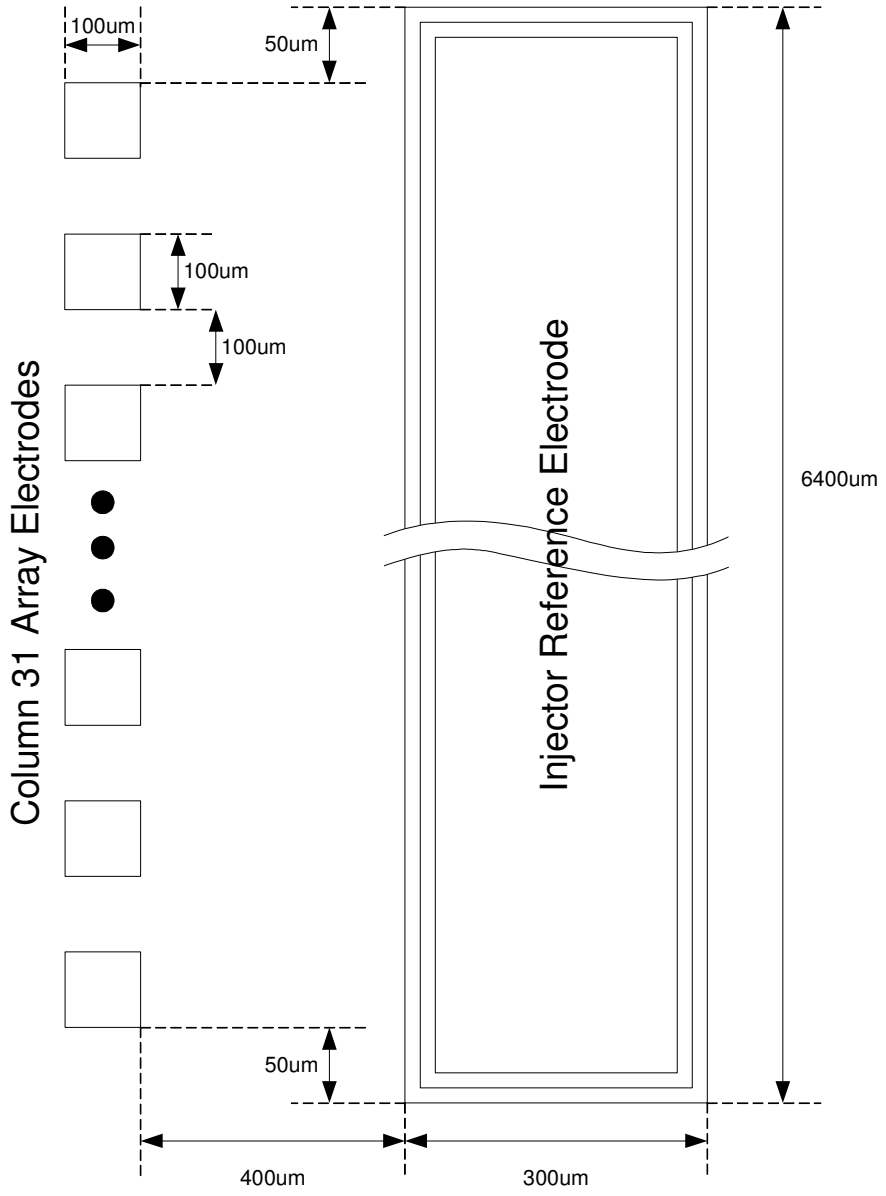


Figure 4-26 Top view of the injector reference electrode relative to the column 31 electrodes

The top view dimensions of the reference electrode and column 31 electrodes are shown in Figure 4-26. The metal 1 and poly layers of the reference electrode have a total vertical length of 6400um and a horizontal width of 300um. The top M3 layer is slightly smaller with a vertical length of 6394um and horizontal width 294um. The M3 layer is spaced 403um away from the M3 layer of the injection electrode side. The electrode is routed through its metal 1 layer from the lower end, which leads out to a pogo pin and

bond pad, controlling the electrode's voltage output. The injector reference electrode has no control circuitry and is directly controlled through a pad to allow flexibility in its output. As a result, in studying droplet injection, any arbitrary AC or DC signal can be applied to it.

4.7.3. Injection Three-state Circuitry

Operation and Addressing Scheme

To support injection, the column 31 (COL31) electrodes need the additional functionality of a 0V ground state. To add this functionality to each cell in column 31, an additional column of cells, each composed of a high-voltage pull-down transistor, data memory and enabling logic is added to the driver array. This column of addressable pull-down drivers is called the injector column or COLINJ. For each COL31 cell, there is a corresponding COLINJ cell.

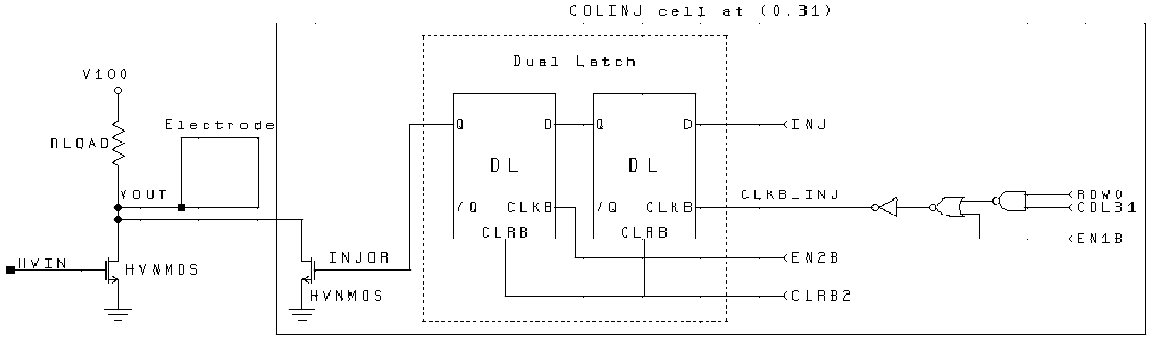


Figure 4-27 Schematic of the COLINJ cell connected to output of its corresponding COL31 electrode

A schematic of the COLINJ cell is highlighted by the solid box shown in Figure 4-27. To the left of the COLINJ cell is the high-voltage transistor, resistor load and electrode of the corresponding COL31 cell. The COLINJ cell is composed of a pull-down transistor whose drain is connected to the output of the adjacent COL31 cell and forces the output

to ground when turned on. The gate of the pull-down transistor is controlled by its own dual-latch memory that receives data from an externally supplied INJ signal. All COLINJ cells receive data from the INJ input rather than from the D phase data from the shift register. The COLINJ cell shares the same address as its corresponding COL31 cell and is reset and enabled through the same control signals. If INJ is logic high when the corresponding COL31 is programmed, once the array is updated, the output of the COLINJ memory INJOR will become logic high, the pull-down transistor will turn on, and the output of the COL31 electrode will drive to ground. However, if INJ is set to logic low when the corresponding COL31 cell is programmed, INJOR will be logic low, the pull-down transistor will to remain off and the COL31 cell will operate normally.

Simulation of the Activated Ground State

The timing diagram for the activation of the ground state on cell (0,31) is shown in Figure 4-28. The figure illustrates the signals needed to operate the COLINJ cell. First, the CLRB1 and CLRB2 signals are deactivated. Then, the row and column addresses of cell (0,31) are clocked into the shift register through the DATA_IN input. Setting the D data bit in the serial input data is not necessary since this will not affect the activation of the ground state. Once the address data is stored, the LOAD signal is activated, passing the addresses to the decoders. The EN1B signal is then activated, and the logic high INJ data is stored into the input latch of the COLINJ cell's memory. Then, the EN2B signal is activated, updating the output latch of the COLINJ cell's memory. The pull-down transistor turns on and drives the 100V square-wave output of cell (0,31) to ground. The

COLINJ memory element resets to logic low when the active low CLRB2 is logic low, restoring the 100V square-wave at the electrode output of COL31.

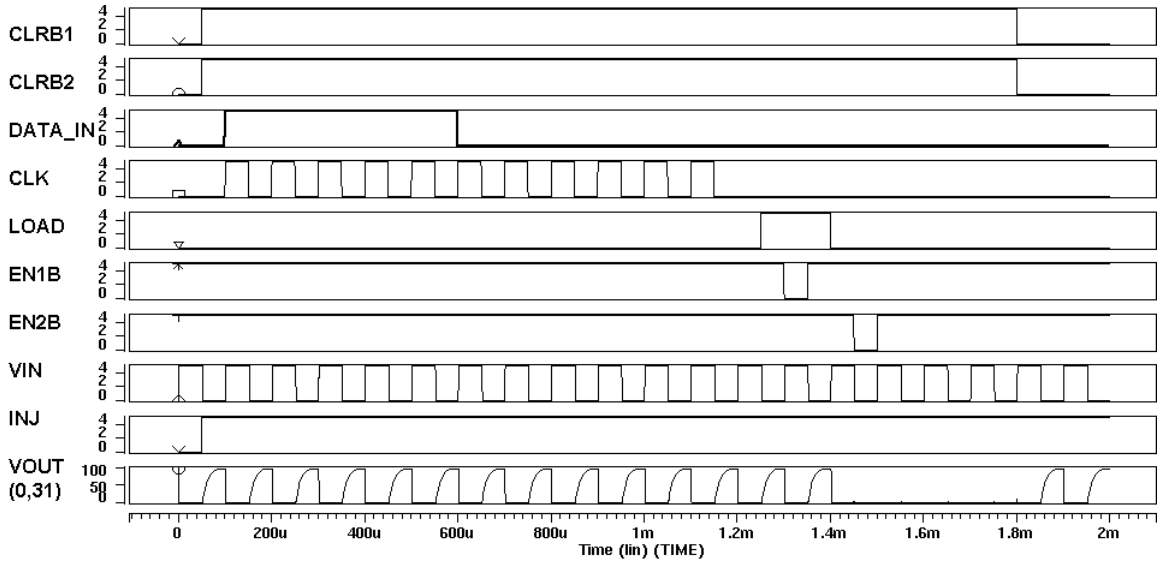


Figure 4-28 Timing diagram for activation of ground state on cell (0,31) from HSPICE

4.8. Chapter 4 Summary

In this chapter, the details of the PFP IC circuitry are given. An overview of the PFP IC inputs and the programming operation is described in 4.1. A detailed analysis of the 1-bit latch building block and its configuration for use in the memory elements of the shift register and the driver cell is given in 4.2. In 4.3, the shift register is discussed and its functionality is verified by experimentation. The digital driver, its component parts and the arrangement of the driver cells to form the array are illustrated in 4.4. Based on experiments of the digital driver test cells, it is shown that the driver cell is capable of generating the high voltage output and can be programmed to the desired phase state. In 4.5, the 5-bit address decoder is described and its functionality is verified experimentally by enabling a set of the decoder output monitor lines. In 4.6, the design of the buffers for the intermediate signals with large fan-out is described, and performance simulation

results are given. The specifications of the buffers are stricter than what is required and the resulting designs meet or are very close to meeting the optimization goals. Although no particular tests are designed for the buffers, verifying the successful operation of the system components demonstrates that the buffers are working properly. Finally, in 4.7, the injection column circuitry and how it is designed to meet the requirements given by the UTMDACC for DEP-assisted droplet injection is discussed.

In the next chapter, the test setup, test procedure and experimental results of the PFP IC will be presented and discussed.

References

[1] J. Vykoukal, J. A. Schwartz, F. F. Becker and P. R. C. Gascoyne, "A Programmable Dielectrophoretic Fluid Processor for Droplet-Based Chemistry," Micro Total Analysis Systems 2001, A. van den Berg et al. (eds), Kluwer Academic Publishers, The Netherlands, pp 72-74, 2001.

Chapter 5 PFP IC Testing, Data and Discussion

In this chapter, the experimentation of the PFP IC will be described. First, details of the test setup and the experimental procedure will be given. Following that, experiments conducted by UC Davis on the electrical capabilities of PFP1K will be discussed. The experiments test the capability of the communications circuitry, the standard driver cell circuitry as well as the injection circuitry. Some non-ideal effects such as probe loading and premature updating of the output phase observed during testing will be explained. Finally, a test conducted by the UTMDACC illustrating PFP1K's capability to induce droplet movement will be discussed.

5.1. Electrical Testing Performed by UC Davis

5.1.1. Test Setup and Signal Generation

Requirements

Since the PFP IC requires at least 8 control signals for normal operation, a DAS9100 digital analysis system capable of generating multiple arbitrary waveforms is used. A series of standard power supplies are connected in series to generate the high voltage supply voltage. Due to the high number of electrode outputs on the PFP1K, bonding them to package pins is impractical. Instead, no special wiring of the outputs is performed on the layout and the high voltage outputs of the system are probed from the top of the chip by microprobes. A Micromanipulator manual probe station model HS 6000 is used to probe the electrode outputs of the chip. An interface board designed to route the chip inputs, power and monitors to a protoboard, while allowing the chip to be

probed from under the microscope is used. The interface board is built by Mike Banducci of UC Davis. In addition, the test setup is designed to accommodate both the PFP1K and the PFP31119 chips to reduce the amount of testing hardware required.

Chip packaging and interface hardware to allow for the probing of the chips

To allow direct probing of the chip, open top packages are used. The PFP31119 uses the open top package type CQFP80. However, the CQFP80 package requires an adapter that routes the package pins into PGA type pins. The adapter applies a clamping force on the chip to ensure connections from the pins to the adapter. However, the same mechanical clamp obstructs access of the chip from the top. As a result, the top of the adapter was shaved to remove the obstructing adapter lid. The PFP1K chip is packaged in an open top 180-pin PGA package, which inserts directly into a PGA socket and therefore does not require the use of a separate adapter.

All chips have a clear oxide layer that covers and seals in the layers of the chip called the passivation layer. Normally, this layer prevents probing of the electrodes on the M3 layer. However, PFP31119 has passivation holes at the electrode locations to allow probing of the M3 electrodes. PFP1K does not have these passivation holes since PFP1K was treated as the final version for the prototype system and the complete oxide layer is left in place. As a result, probing of PFP1K's electrodes is performed by first scraping off the oxide at a particular electrode location using the sharp microprobe tip to access the M3 layer. The oxide scraping and probing process is not a perfect process and the

results can vary for each case. However, it is sufficient enough to verify the periodic signal at the output, the output magnitude and any phase changes in the output.

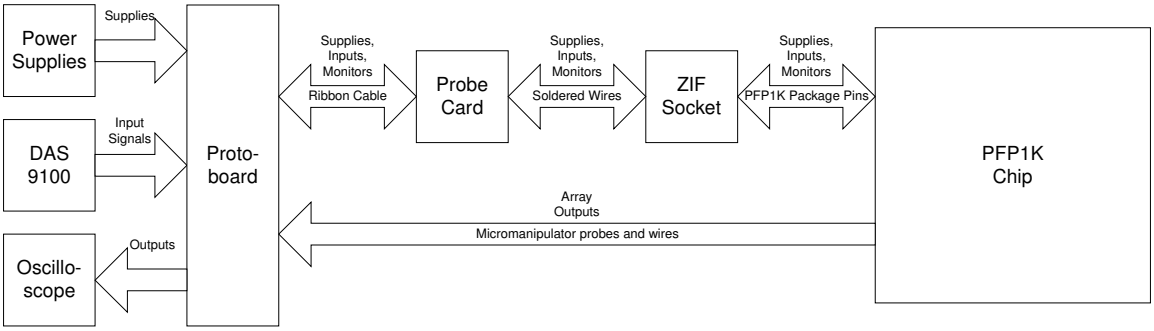


Figure 5-1 Test interface of the PFP1K chip

The test interface for PFP1K is illustrated in Figure 5-1. The power and input signals are first routed to a protoboard, which connects to DIP connectors on the probe card via ribbon cables. The probe card is fastened under the micromanipulator station and has a PGA ZIF socket for the chip under testing. The signals entering through the DIP connectors on the probe card are routed to the ZIF socket, where the chip is to be seated. Since PFP1K chip uses a PGA package, it plugs directly in the PGA ZIF socket, while the PFP31119 chip is first placed within an adapter, which then plugs into the PGA ZIF socket. For each test chip version, there is a separate set of DIP connectors on the probe card. Output signals taken by microprobes are routed directly back to the protoboard where is it probed by an oscilloscope.

Test input generation and data acquisition

The PFP IC system is tested by programming a selected array driver cell and monitoring its electrode output for phase changes and high voltage capability. The required input and control signals for a programming cycle are first simulated in HSPICE with the PFP

IC system's communications circuitry connected to a single digital driver cell at the target address. Once the programming cycle has been successfully simulated, the input waveforms are programmed as logical values into the DAS9100, which is capable of producing multiple arbitrary logical waveforms. The DAS9100 is set up to only produce the inputs to the PFP IC and not to read in any signals. When the DAS9100 pattern generator is activated the DAS9100 produces the entire pattern of logic values and repeats it periodically. Thus, each signal during an entire programming cycle can be displayed on the oscilloscope screen. Because many signals are required to operate the PFP IC, they cannot be probed and saved simultaneously. Instead, they are probed one-by-one, saved onto disk and then plotted together in Matlab.

5.1.2. PFP IC System Functional Testing

5.1.2.1.Communications and Non-Injection Driver Circuitry Testing

PFP1K's communications circuitry and digital driver circuitry are tested for functionality at a 100Hz operating frequency and high voltage supply of 5V. The PFP1K's system is tested for three cases that verify the correct operation of the circuit components. In the first test, the phase transition from out-of-phase to in-phase is tested by programming a driver cell memory with a logic high input data bit. In the second test, the phase transition from in-phase to out-of-phase is tested by programming a driver cell memory with a logic low input data bit. Since all memory elements are initialized to a logic low data and thus all outputs initialize in the out-of-phase output state, the target cell is first programmed with a logic high data before being programmed with the logic low data. In the third test, the simultaneous output update function is tested. Two cells are

sequentially programmed with a logic high data bit. Only after the second driver is programmed is the output updated. Both driver outputs should change phases from out-of-phase to in-phase simultaneously. The three experiments and their results are discussed next.

Case 1: Programming a driver cell with a logic high phase data

The first test demonstrates the driver cell's capability to read in a logic high data bit and output that data and is performed by programming a driver cell to change its output phase from 180-degrees (logic low phase data) to 0-degrees (logic high phase data) in phase with the reference signal. The input and output waveforms for this experiment are shown in Figure 5-2. The target cell is the digital driver cell at row 1 and column 30 or (1,30) and its phase data bit is logic low upon reset. At time t=0.0025s, the CLRB1 and CLRB2 signals are deactivated and the system is ready for programming. Between t=0.01s and t=0.12s, the binary data for column 30 and row 1 addresses and a logic high phase bit are loaded into the shift register and then passed to the other parts of the circuit by the LOAD signal at time t=0.1225s. The 1-bit phase data is sent to all driver cells, while the addresses are decoded, enabling the driver cell with the target address. At time t=0.1275s, the EN1B signal is pulsed and the input latch of the target cell's memory reads in the logic high phase data bit. The EN1B signal is stopped at t=0.1325s and the LOAD signal is deactivated at time t=0.1375s. At time t=0.145s, EN2B is pulsed and the output latch is updated with the new phase data. The output VO1X30 changes phases from 180-degrees to 0-degrees in phase with the reference signal VIN. Finally, at time

t=0.1775s, CLRB1 and CLRB2 are enabled and the system is reset, reinitializing the output phase to be 0-degrees in phase with the VIN reference signal.

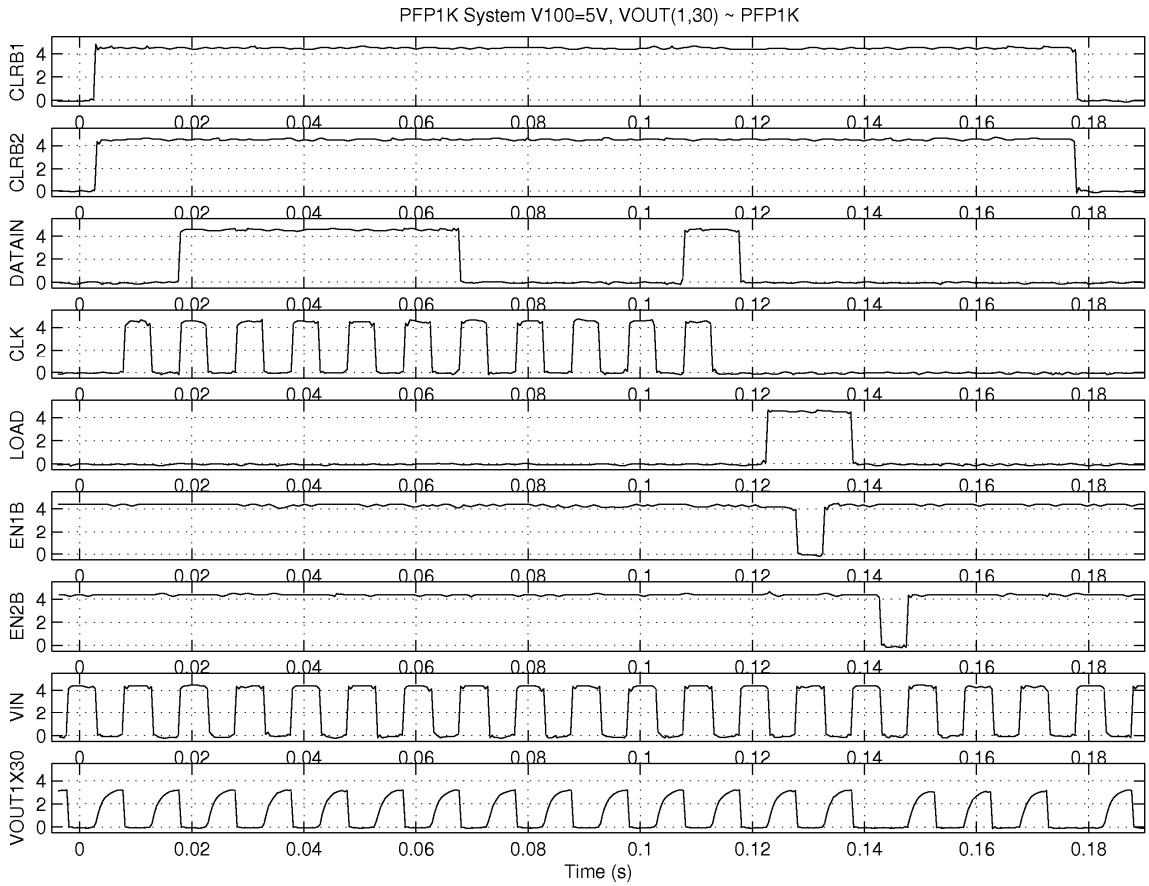


Figure 5-2 PFP1K system functional test of a 0→1 phase data program on cell (1,30) of PFP1K chip at V100=5V. The output updates when EN2B is enabled at time t=0.143s

The functionality of the communications circuitry and the phase change capability of the full-sized PFP IC system is verified at f=100Hz and V100=5V. The output changes phase exactly when EN2B is pulsed and resets when CLRB2 is enabled. Notice that the logic high output of the digital driver is about 3V, significantly lower than the high voltage supply of 5V used here. This output attenuation is due to a probe loading effect caused by the large output resistance of the digital driver and type of probe used to

measure the output. The probe loading effect is present on all output waveforms taken from the PFP test chips and is discussed in detail in Chapter 5.1.4.2.

Case 2: Programming a driver cell with a logic low phase data

In the next test, the digital driver cell's ability to read in a logic low data input and to set the output phase from 0-degrees to 180-degrees in phase is demonstrated. Since upon reset, a logic low data is present in all digital driver cells, the target cell needs to be first programmed with a logic high data bit before being able to monitor an output phase change during a logic low programming cycle. Therefore, in this experiment, a driver cell is first programmed with a logic high phase data bit to create a 180-degree to 0-degree output phase transition. Then, the same driver cell is programmed with a logic low phase data bit to observe the 0-degree to 180-degree output phase transition.

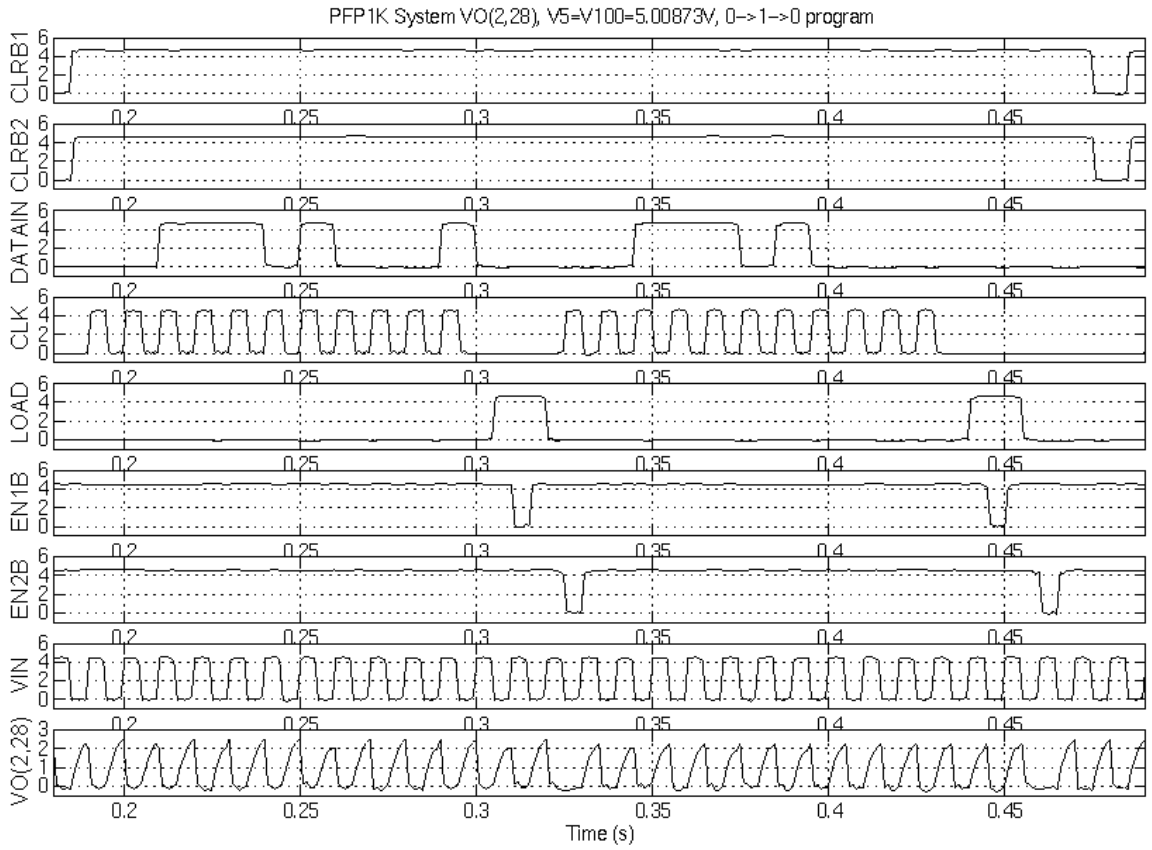


Figure 5-3 PFP1K system functional test of a 1→0 phase data program on cell (2,28) at V100=5V. A 0→1 program is first performed, followed by the 1→0 program. The output is updated from 0→1 at t=0.325s and from 1→0 at t=0.46s

The driver cell used here is cell (2,28) and the test waveforms are shown in Figure 5-3. The reset is deactivated at t=0.185s and the eleven data bits composed of addresses and logic data are passed into the shift register from t=0.190s to t=0.300s. At time t=0.305s, the LOAD signal is activated, passing the data from the shift register to the decoders and array, and at t=0.310s, the EN1B signal is activated, commanding the target cell to latch in the logic high data. At t=0.325s, the EN2B is activated and the output changes phases from 180-degrees to 0-degrees. Immediately following that, eleven new data bits targeting the same address but with a logic low phase data bit are loaded into the shift register from t=0.325s to t=0.435s. The LOAD signal is activated at t=0.440s and EN1B is activated at t=0.445s, latching the driver cell memory with a logic low data. At time

t=0.460s, EN2B is enabled a second time and the output square wave is updated with the logic low data, changing the output from 0-degrees back to 180-degrees in-phase with the VIN signal. At time t=0.475s, the memory is reset, but the output of the digital driver is unchanged as it already contains a logic low phase data. The experiment shows that the system is capable of programming a driver cell to both phases.

Case 3: Programming two drivers sequentially and updating their outputs simultaneously

In the third case, the simultaneous update feature is demonstrated. In the previous two experiments, the EN2B signal is pulsed and the outputs updated immediately after the input latch of the target cell stores the input phase data. In this experiment, two adjacent cells are sequentially programmed with a logic high data bit and then simultaneously updated once both cell memories have the new phase data stored in their input latches. The first cell is programmed with a logic high data bit and immediately after, another cell is programmed also with a logic high data bit. Only after the second cell is programmed is EN2B pulsed and the output of both programmed cells updated with the logic high phase data.

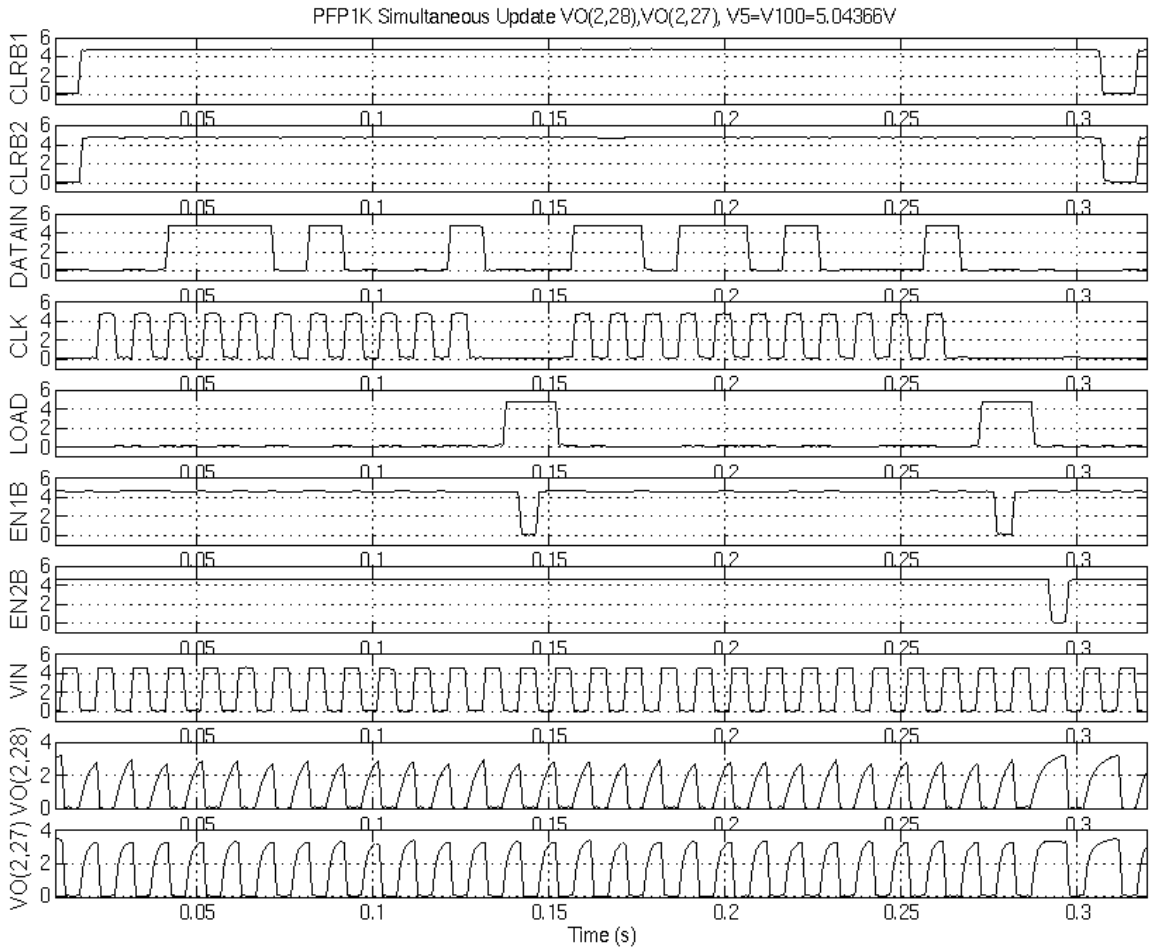


Figure 5-4 PFP IC system output update test at V100=5V demonstrating a sequential programming of two adjacent cells, (2,28) and (2,27), and then a simultaneous update of their output phase at t=0.291s

The two adjacent cells that are programmed sequentially and then updated simultaneously are at (2,28) and (2,27) and the test waveforms are shown in Figure 5-4. At time t=0.017s, the CLRB1 and CLRB2 are set to logic high. The shift register receives the address and logic high phase data for cell (2,28) between t=0.022s and t=0.132s. After that, LOAD is pulsed from t=0.137s to t=0.153s and EN1B is enabled from t=0.141s to t=0.147s, loading the logic high data into the cell's input latch. From t=0.157s to t=0.267s, the shift register loads in the address and logic high phase data for cell (2,27). At time t=0.138s, LOAD is set to logic high and the shift register data is

passed to the rest of the circuit. At t=0.142s, the EN1B is activated and the memory at cell (2,27) loads in the logic high phase data. The EN2B is enabled at t=0.292s and the outputs of both (2,27) and (2,28) are updated. The outputs of both (2,27) and (2,28) show a phase change from 180-degrees to 0-degrees at t=0.292s as expected. The system is reset at t=0.307s and the outputs of (2,27) and (2,28) are set back to the 180-degrees in-phase state. This experiment successfully demonstrates the controlled, simultaneous output update by the EN2B signal.

5.1.2.2.HV Output Probe Loading Effect

The output attenuation observed in the driver cell outputs is due to a probe loading effect caused by the output resistance of the digital driver and the resistance of the scope probe. The scope probe used is a passive attenuator type 10Mohm probe, which in most cases has a sufficiently high resistance. However, the output resistance used in the digital driver is 5Mohm, half of the probe resistance, which results in a voltage division that significantly reduces the output amplitude when probing the circuit. In this section, the probe loading effect and the maximum output voltage at the oscilloscope input are verified through a hand analysis and simulation of the high voltage NMOS, scope probe and oscilloscope load and through further testing of the high voltage cell outputs.

Hand analysis and simulation of the scope probe model

The output level of the digital driver connected to the oscilloscope through the 10Mohm scope probe is analyzed here. The probe used to measure the high voltage output of the digital driver is a Tektronix P6009 probe with 100:1 attenuation. The equivalent probe

model taken from [1] and the oscilloscope input impedance of the HP54522A oscilloscope connected to the high voltage output of the digital driver NMOS transistor is shown in Figure 5-5a.

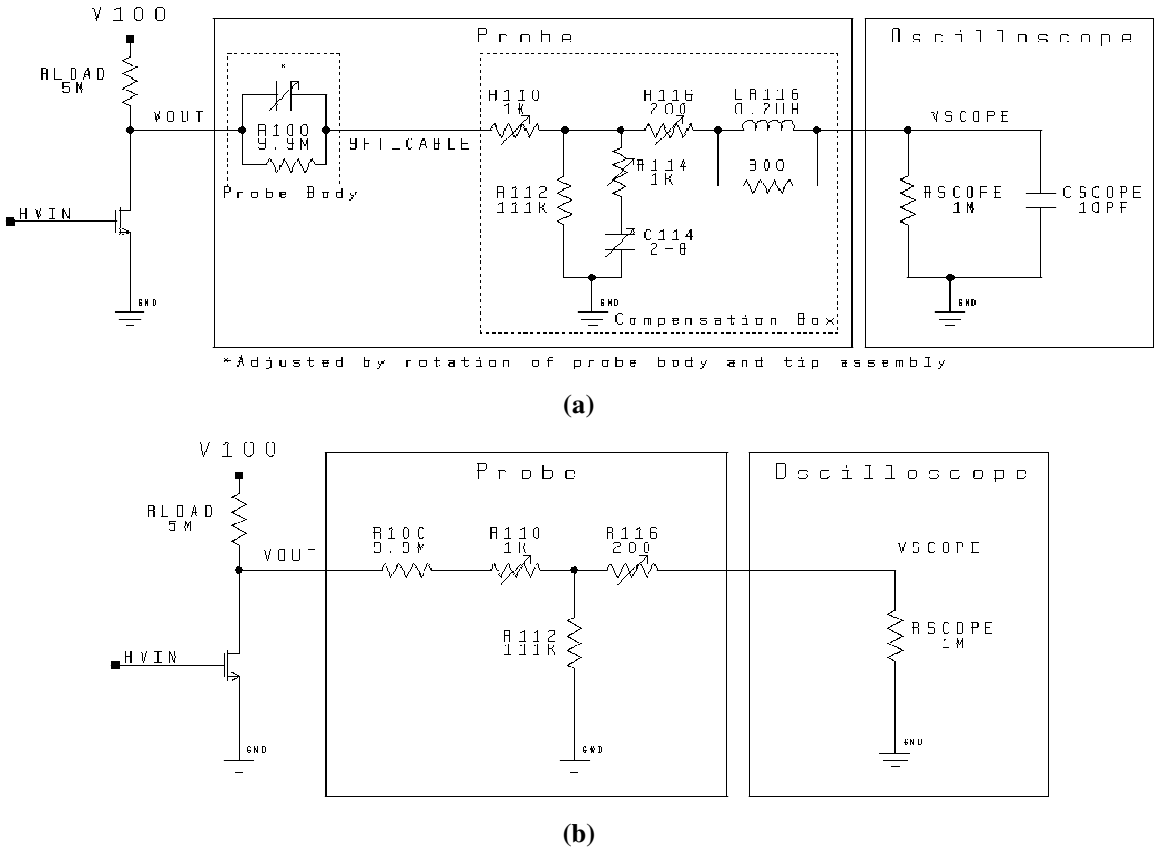


Figure 5-5 Schematic of the oscilloscope connected to the digital driver output using (a) a full schematic representation of scope probe and (b) a resistor-only representation of the scope probe and oscilloscope

At DC, the capacitances shown in Figure 5-5a are open and the resulting resistive network is shown in Figure 5-5b. In the general case where probe loading is not an issue, for example when the NMOS transistor is turned on and VOUT is a voltage close to ground, the voltage seen at the oscilloscope input is equal to

$$V_{SCOPE} = \left(\frac{R_{SCOPE} R_{112}}{(R_{100} + R_{110} + R_{112})(R_{SCOPE} + R_{116}) + (R_{100} + R_{110}) R_{112}} \right) V_{OUT} = 0.009988 * V_{OUT},$$

which confirms the 100X attenuation of the scope probe. However, when the NMOS transistor is turned off, the voltage at the probe tip is driven by the V100 supply through the 5Mohm RLOAD resistor and the voltage seen at the oscilloscope input is

$$\begin{aligned} V_{SCOPE} &= \left(\frac{R_{SCOPE} R_{112}}{(R_{LOAD} + R_{100} + R_{110} + R_{112})(R_{SCOPE} + R_{116}) + (R_{LOAD} + R_{100} + R_{110}) R_{112}} \right) V_{100} \\ &= 0.006659 * V_{100} \end{aligned}$$

The result shows that the maximum voltage at the oscilloscope input at a V100=100V supply is VMAX=66.59V under probe loading conditions and when taking into account the 100X attenuation.

HSPICE simulations of the resistively loaded HV NMOS output connected to the probe and scope models are shown in Figure 5-6 for V100=5V and V100=100V. A 100Hz 5V square wave is applied to the gate of the HV NMOS. The peak voltage output is about 3.32V for the V100=5V case and 66.5V for the V100=100V case. The output is limited to about two-thirds of the supply voltage in the simulation, confirming the results of the hand analysis and the observations made in the PFP IC experiments.

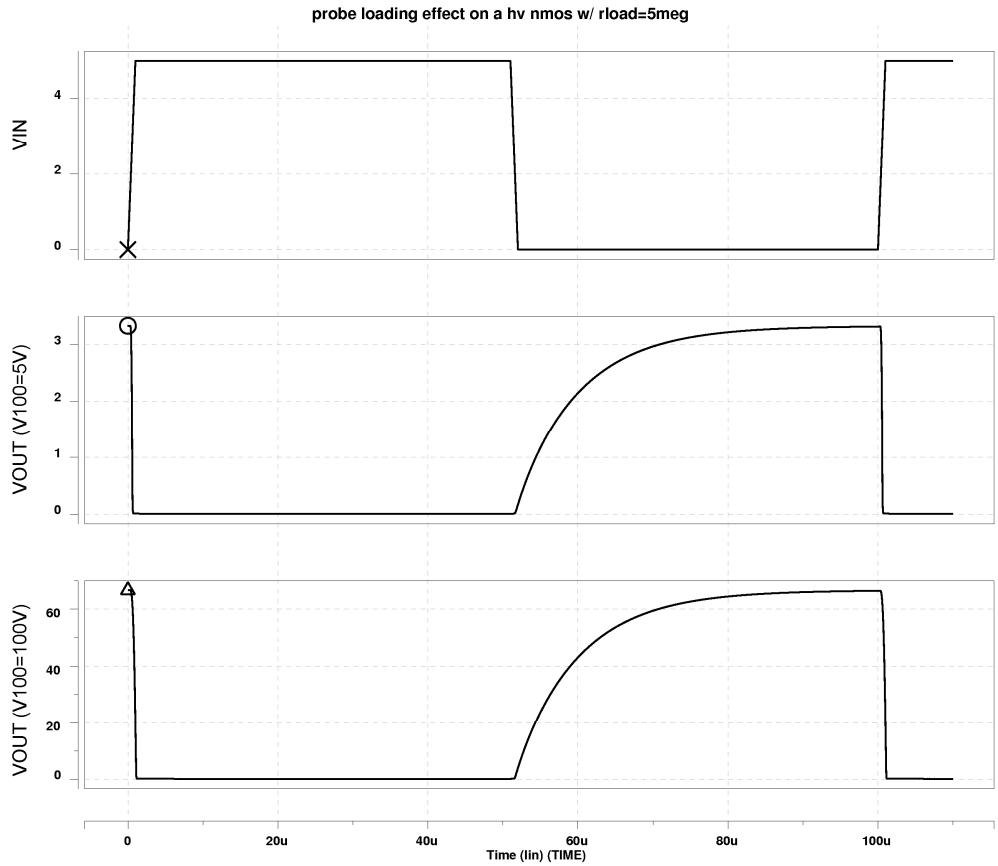


Figure 5-6 HSPICE simulation of the oscilloscope input voltage from digital driver output HV NMOS connected through the probe model for V100=5V and V100=100V

Experimental measurements of the output voltage level

The probe loading phenomenon is further studied by programming phase changes at various V100 values. The cell at location (1,30) is tested at V100=40V, 60V and 80V and the digital driver outputs are shown in Figure 5-7. In all cases, the peak digital driver output is about two-thirds the value of the V100 supply and often times slightly lower than that. The experiment is repeated on cell (2,29) for V100=80V and 100V as shown in Figure 5-8 and the same probe loading effect is seen there.

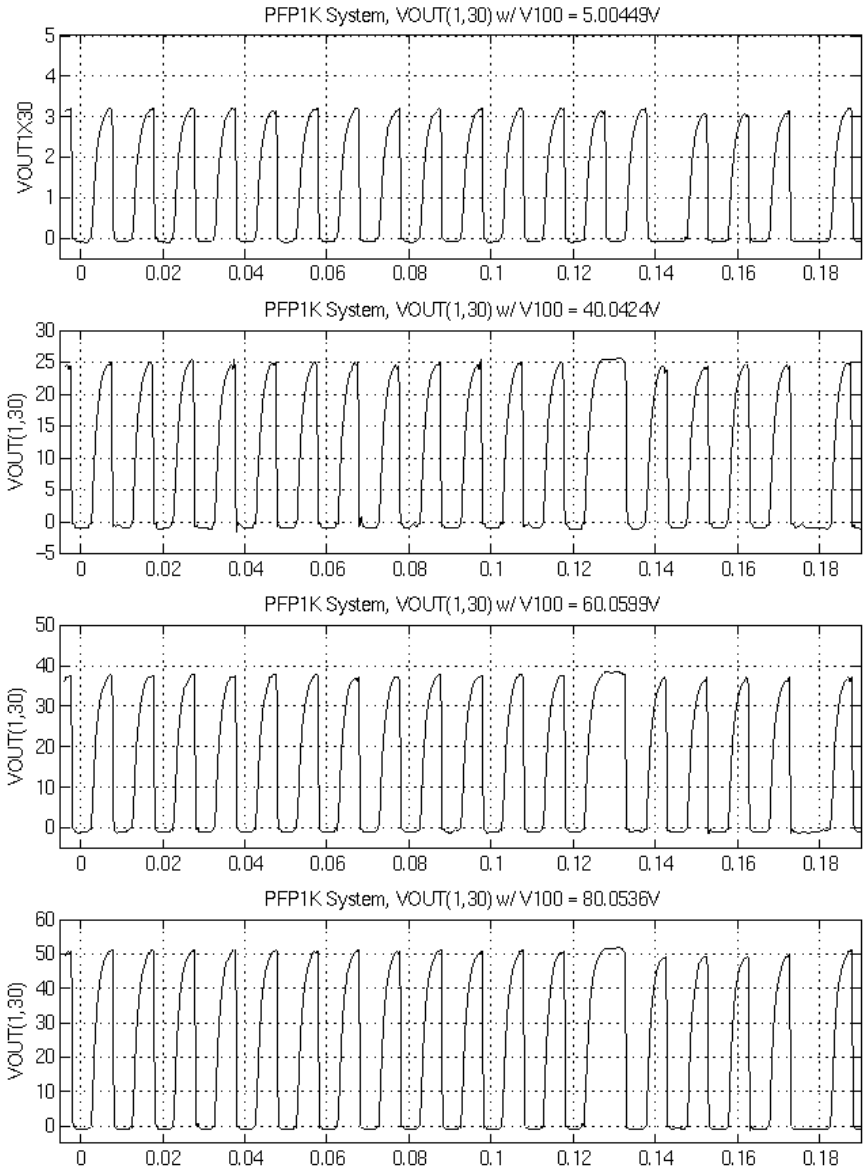


Figure 5-7 The voltage output of the digital driver cell at (1,30) performing a phase state change and reset for V100=5V, 40V, 60V and 80V

From five different experiments using five different test cells over a variety of supply voltages, the average, minimum and maximum peak voltages are calculated. The average peak output is 65.0447%, the minimum is 59.4549% and the maximum is 69.5506% of the V100 supply voltage. The results do not vary much in terms of supply voltage, but do vary between differing cells. This might be attributed to the oxide scratching process

used, which may have affected performance of some of the cells, or the non-ideal off-resistance of the HV NMOS in parallel with the probe impedance.

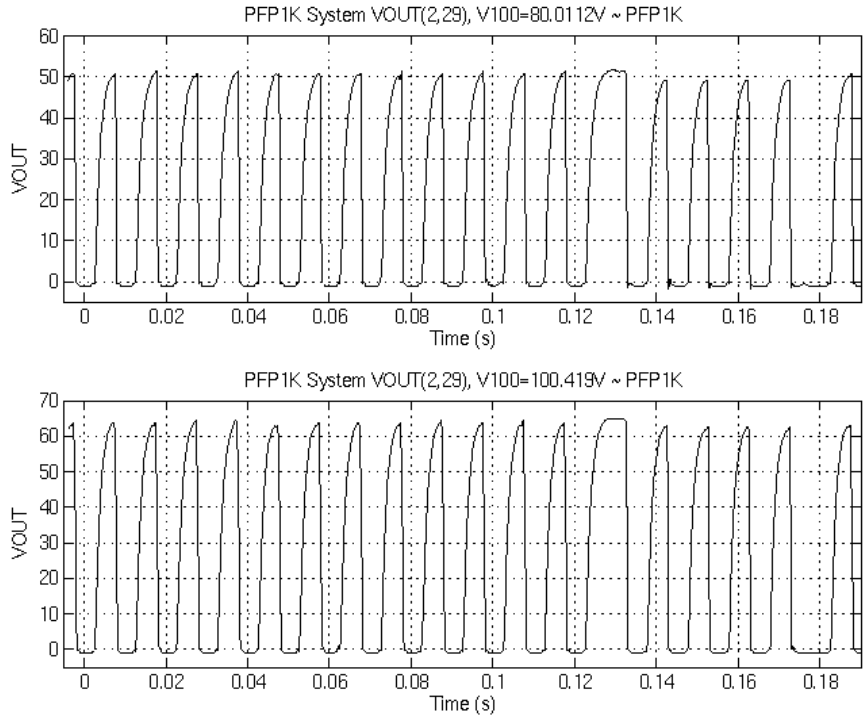


Figure 5-8 The voltage output of the digital driver cell at (2,29) performing a phase state change and reset for V100=80V and V100=100V

In these tests, another strange effect is observed as the high voltage supply is increased. Notice that in tests where V100 is greater than 5V shown in Figures 5-7 and 5-8, the update of the phase output occurs earlier than in the 5V case although EN2B activates at the same time in all cases. This premature updating of the new phase data will be discussed next.

5.1.2.3.Investigation of the Premature Output Update

From tests conducted at voltages greater than the 5V supply, the output phase updates with the new phase data earlier than expected, implying a relationship between this

premature update and the high voltage supply V100. At 5V, the output updates appropriately when EN2B is enabled. However, as the V100 supply is increased, the output updates before EN2B is pulsed as seen by comparing the output for the V100=5V case and the V100=40V case shown in Figure 5-7. In the V100=40V case, the output update is 1.5 clock cycles earlier than the V100=5V case.

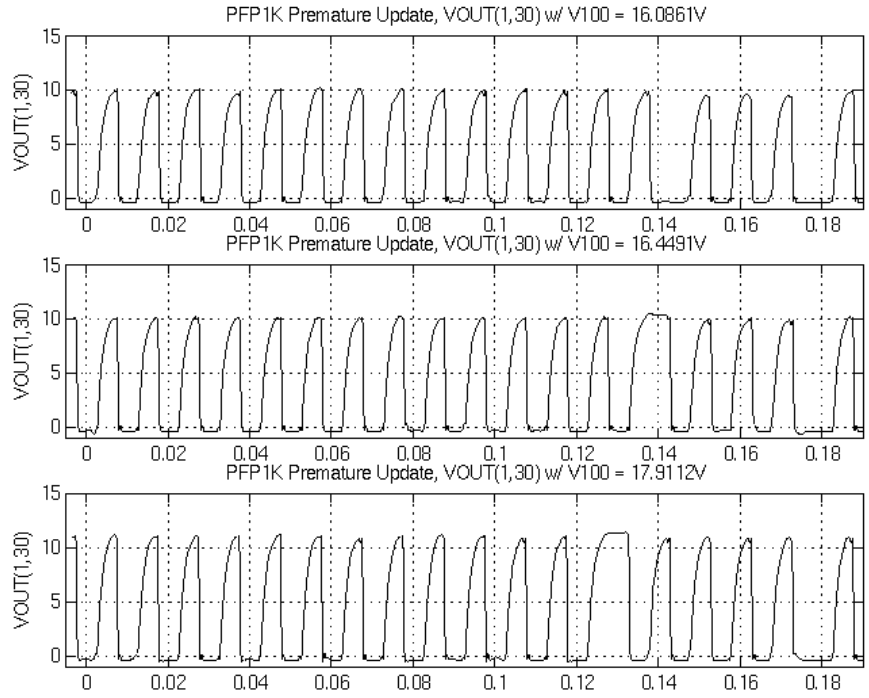


Figure 5-9 Timing diagram illustrating the premature output update for V100=16.0861V, 16.4491V, and 17.9112V at which the phase change shifts from the correct time (t=0.145s) to the incorrect time (t=0.125s)

To investigate this problem, the V100 is slowly increased from 5V until the output shows signs of an early update during a normal programming cycle. The test uses the same programming sequence as Case 1 in Chapter 5.1.2.1. The output should update when EN2B is enabled low at around t=0.142s. At V100=16.0861V and below, the output update still occurs at the correct time as shown in Figure 5-9. However, at V100=16.4491V, the output update occurs half a clock cycle early. Instead of holding

the 0V output for an entire period during the phase transition, the preceding 100V output is held for an entire period. At V100=17.9112V and beyond, the output updates even earlier at 0.128s, which is 1.5 periods earlier than when EN2B is activated.

The test setup is suspected to be the reason for the premature update but this is difficult to verify. The test setup has shown faulty operation in a previous experiment, where some signals connected to the chip appeared and disappeared from the oscilloscope during probing. There, it was found that when the ZIF socket lever was all the way down, some signals did not appear on the oscilloscope, whereas when it was only halfway down, all signals were present.

Although it is difficult to determine the exact suspect for this effect, control of the output update can still be verified. As long as the output can be updated in a controlled fashion through EN2B, an early output update will not affect the desired operation of the chip. To verify a controllable output update, the chip is tested under a normal programming sequence with and without pulsing EN2B at V100=5V and 20V. At V100=5V, no early output update should be observed when the EN2B signal is pulsed and no update should occur unless EN2B is pulsed. At V100=20V, however, an early output update will be observed when the EN2B signal is pulsed, but the output update should still not occur unless EN2B is pulsed.

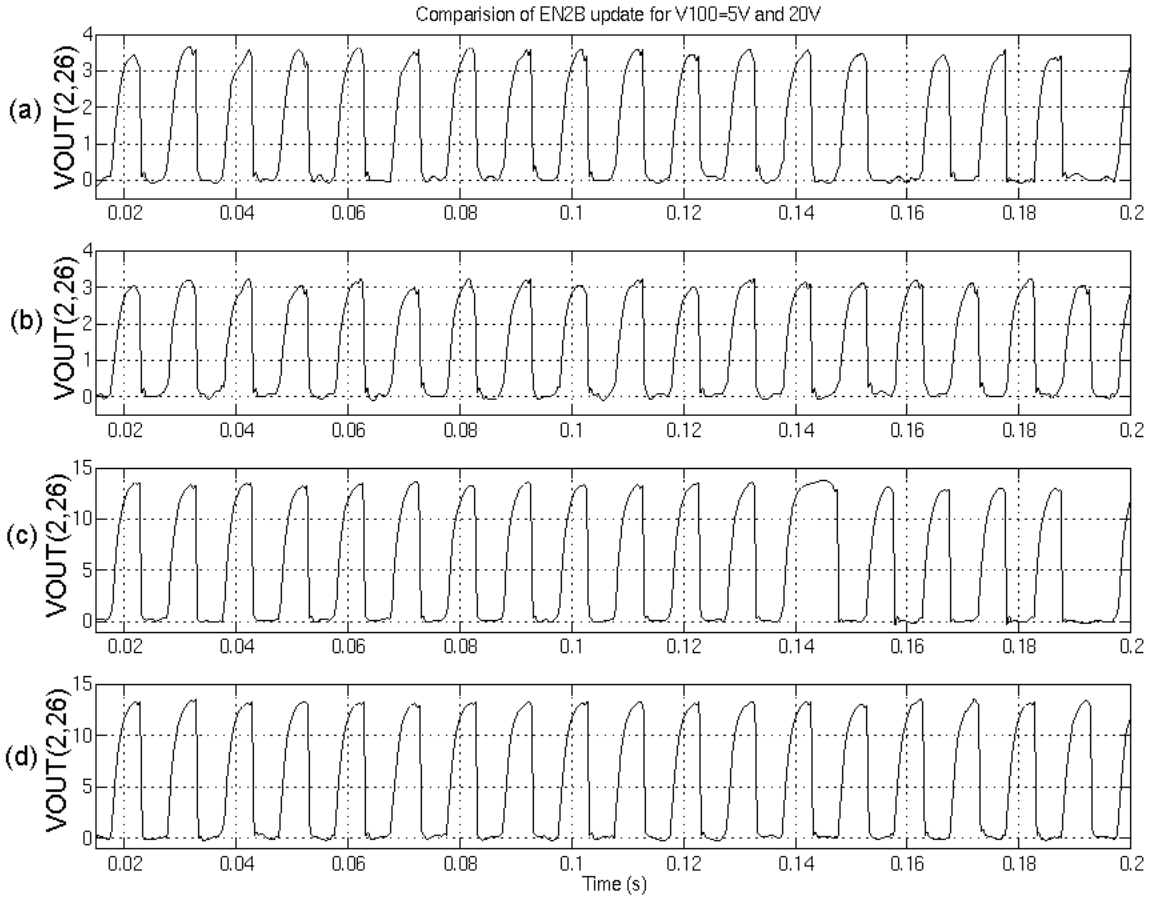


Figure 5-10 Comparison (a)V100=5V and EN2B is enabled at t=0.1575s (b)V100=5V and EN2B is not enabled (c)V100=20V and EN2B is enabled at t=0.1575s (d)V100=20V and EN2B is not enabled

The EN2B control of the output update is tested on cell (2,27) and the results of the experiment are shown in Figure 5-10. In Figure 5-10a, V100=5V and the output changes phases at about time t=0.1575s. In Figure 5-10b, the EN2B signal is not pulsed at all and the output does not change phases as expected. In Figure 5-10c, V100=20V and the 1.5 clock cycle early output update is again observed, however, in Figure 5-10d, the EN2B signal is not pulsed and the output phase does not change phases as expected. The above experiments verify that although a premature update exists under the given test setup at supply voltages greater than about 18V, the output phase is still controlled through the EN2B signal and does not update unless EN2B is activated.

5.1.2.4.Injection Circuitry Testing

In this section, the COLINJ circuitry is tested for functionality. During programming, when a logic high INJ is latched by a COLINJ cell, the corresponding COL31 cell output should drive down close to zero volts upon the array update. When a logic low INJ is latched, the COLINJ cell should not affect the operation of its corresponding COL31 cell and the corresponding COL31 cell should be programmable through the shift register phase data. Through testing of these two states, (INJ low and INJ high), it is found that the COLINJ circuitry is not working correctly and the COL31 electrodes cannot achieve an acceptable near-ground state. In addition, the COL31 driver cell cannot be programmed to perform phase changes at its output. The cause of this malfunction is a layout error connecting all of the outputs of the COL31 cells together. To illustrate and investigate the problem, two experiments on COL31 cells are performed. In the first experiment, a ground state is attempted by setting INJ to logic high while programming the COL31 cell at location (0,31). In the second experiment, INJ is set to logic low and a 180-degree to 0-degree phase transition is attempted on cell (2,31). Data obtained from the two experiments will first be described and then the incorrect behavior due to the layout error will be explained.

Case 1: Functional test of the COLINJ cell to produce a ground state at COL31

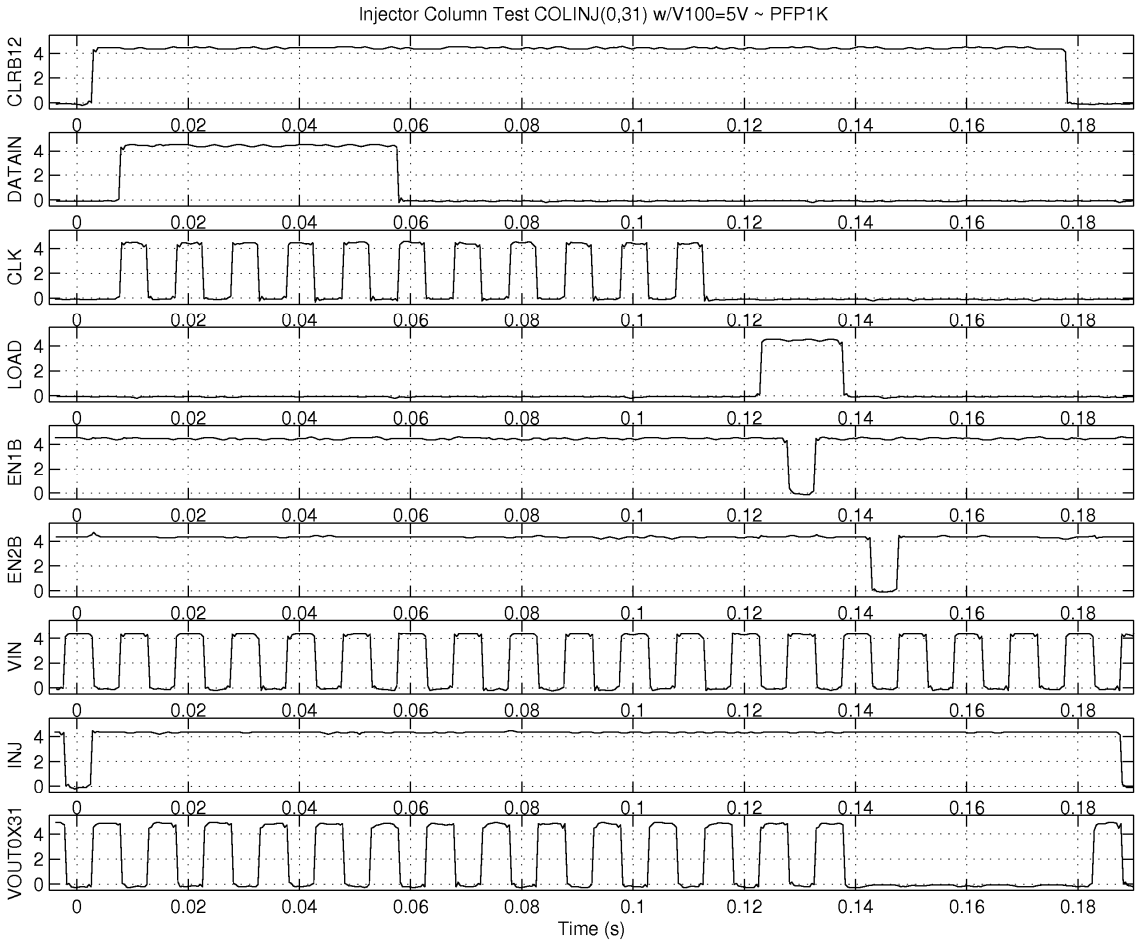


Figure 5-11 Timing diagram for injector column (0,31) test where the pull down mechanism for COLINJ appears to be working properly for V100=5V.

First, the functionality of the COLINJ injection electronics is tested by programming the COLINJ cell at (0,31) with a logic high INJ to pull the output of its corresponding COL31 cell output to ground. The output should be pulled towards ground regardless of the new phase input data in the shift register. The test waveforms are shown in Figure 5-11. At time t=0.00282s, the reset signal CLRB12, which is shared by both CLRB1 and CLRB2 inputs, is deactivated. Between time t=7.865e-3s and t=0.118s, the shift register reads in the cell address for column 31, row 0, and a logic low new phase data bit. Recall

that the COLINJ cell memories are enabled by the same address as their COL31 counterparts. At time t=0.123s, LOAD is activated and the addresses and data are sent out to the respective parts of the chip. EN1B is activated at time t= 0.1279, causing the COLINJ memory to store the injection data INJ, which is logic high. At t= 0.1428s, EN2B is activated and the output of cell (0,31) is pulled down to the ground state output from an 180-degree in-phase square wave by the COLINJ cell. Finally at t=0.1928s, the system is reset and the high voltage square wave is again present at the cell output.

While it seems as though the ground state is working properly, notice the slightly raised voltages faintly resembling four non-zero pulses during the expected ground state time period. In fact, the pulses here are attenuated 180-degree in-phase pulses, showing that the ground state may not be working properly. Also, notice that there is no probe loading effect at the output. The peak output easily goes to the 5V supply unlike in previous tests. In the next test, a COL31 cell is tested for normal phase change operation with the injection cell data set to logic low.

Case 2: Test for a normal phase change of a COL31 cell with the COLINJ cell turned off

The COL31 cell at location (2,31) is tested for normal phase change operation. Since each COL31 cell has COLINJ circuitry attached to it, it is important to test for the phase change capability of the COL31 cell when the injection data INJ is logic low and the COLINJ pull-down transistor is off.

In this experiment, cell (2,31) is tested with a supply V100=100.460V and is performed for both INJ low and INJ high. The control signal sequence is the same as in the previous COLINJ experiment, but using cell (2,31). If a logic low INJ data bit is latched into the COLINJ cell and a logic high phase data is loaded into the shift register, when EN2B is enabled, the output VOUT should exhibit a 180-degree to 0-degree phase transition, and the COLINJ circuitry should not affect the cell's operation. If a logic high INJ data bit is latched into the COLINJ cell, when EN2B is enabled, the output of VOUT should exhibit a 180-degree in-phase square wave to ground state transition.

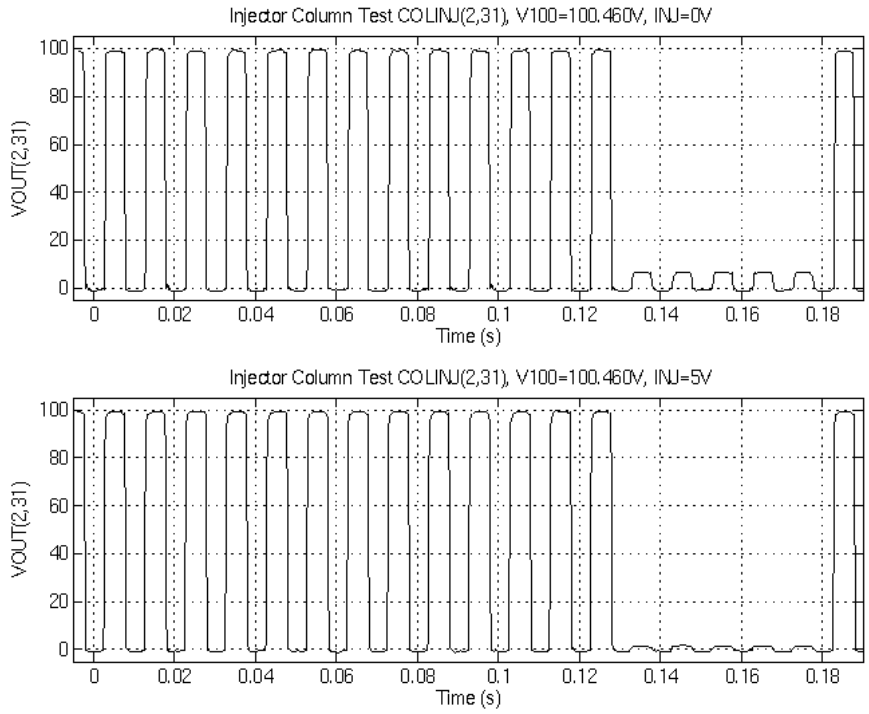


Figure 5-12 Output of driver cell (2,31) while programming a phase change for both INJ=logic low and INJ=logic high. When INJ is logic high, the output is driven close to ground as expected. However, when INJ is logic low, the output is still greatly attenuated when a normal phase shift is expected.

Since V100=100V, the output update will appear earlier that expected as discussed in Chapter 5.1.2.3. As seen in Figure 5-12, when INJ is logic low, the output changes from

a 180-degree in-phase high voltage square wave to a 180-degree in-phase low voltage square wave, rather than a 0-degree in-phase high-voltage square wave. These pulses are non-negligible as there is a very obvious square wave present, showing that the driver cannot perform the phase change function in the presence of the COLINJ circuitry. In the logic high INJ case, the output voltage should change from a 180-degree in-phase square wave to a signal close to ground. However, from Figure 5-12, a non-zero signal resembling a 180-degree in-phase square wave is visible at the output similar to that found in the V100=5V case previously shown. Again, also notice that there is no probe loading in the output signal when there should be as discussed earlier.

5.1.2.5.Investigation of the Malfunctioning Injection Circuitry

Experimentation

The experiment is performed on another driver cell at various V100 supply voltages to verify that the anomalous attenuated square wave during the ground state period exists at other COL31 cell outputs and to observe how the magnitude of the anomalous pulses changes with respect to the V100 supply voltage. In this test the same programming sequence from Figure 5-11 is used and the cell is tested at V100=5V, 40V, 60V, 80V and 100V. The output waveforms are shown in Figure 5-13. At V100=5V, the pulse peaks to about 0.1575V during the ground state time period. As V100 increases, the magnitude of these square waves increases significantly and at V100=100V, the peak voltage reaches 27V, greater than one-fourth of the supply voltage. Also, notice again that there is no probe loading effect and the output is capable of the full V100 output.

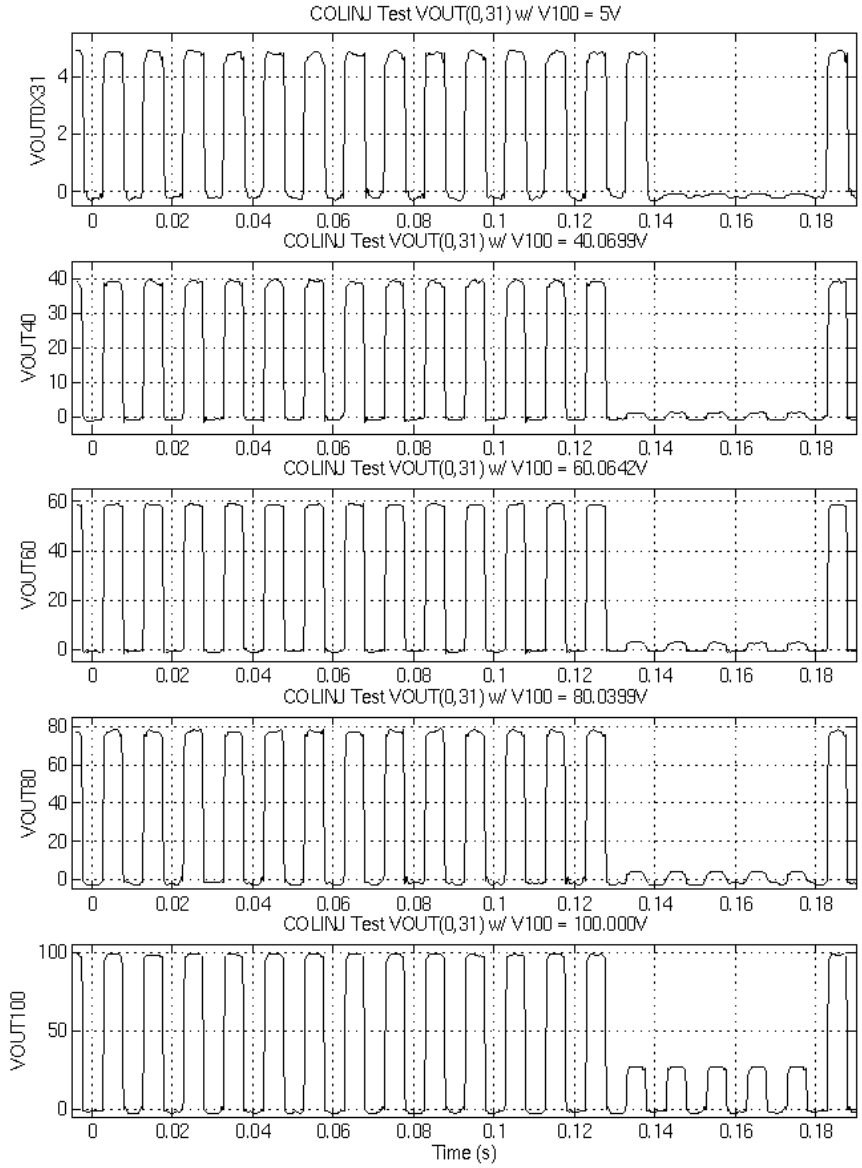


Figure 5-13 COLINJ test with INJ=logic high for increasing V100 showing that as V100 increases, the amplitude of the square-wave during the interval in which it should be close to ground, also increases.

Discussion

The incorrect behavior of the COLINJ circuitry and COL31 circuitry is caused by a layout error shorting all the outputs of the COL31 cells together. The error is illustrated in Figure 5-14, where the COL31 driver cell outputs and the COLINJ outputs are connected to a common node. The figure shows only the COLINJ pull-down transistor

for location (0,31), which will be used for explanation. The faulty behavior of the COL31 output drivers seen in the experiments will be explained using the same two experimental cases seen so far: (1) the INJ data is high, the INJOR signal is logic high and the HV pull-down transistor is trying to pull down the output to ground and (2) the INJ data is low, the INJOR is logic low and a normal phase program of COL31(0,31) cell is attempted.

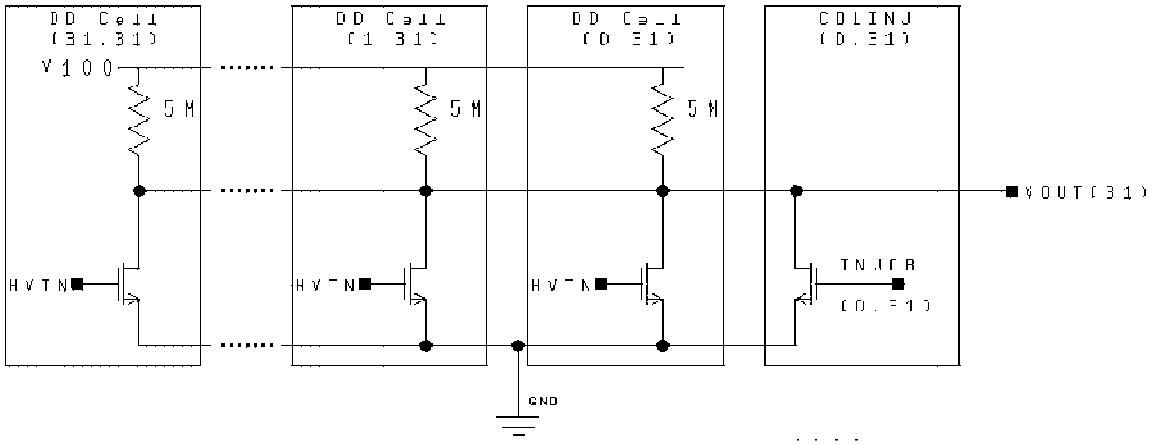


Figure 5-14 Schematic of the COL31 driver cells with outputs tied together and a COLINJ pull down transistor connected to the output.

Case 1: INJOR is logic high and trying to pull down the output

Normally, when the pull-down transistor at COLINJ(0,31) is programmed to drive its output towards ground, it shorts across the source and drain of the high voltage transistor in COL31(0,31). However, since all COL31 outputs are connected here, the COLINJ transistor attempts to short across all 32 high voltage transistors of COL31.

Assuming reset conditions, where there are no phase differences between the COL31 outputs, when VIN is high, all the HVIN go high and the shorted output VOUT(31) should go low. Likewise, when VIN is low, all the HVIN go low and the output

VOUT(31) should go high. When VIN is high while INJOR is high, VOUT(31) is driven towards ground with no problems. However, when VIN is low and INJOR is still high, there is a conflict between the COLINJ pull-down transistor and the COL31 HV NMOS transistors and VOUT(31) cannot be driven down to ground properly.

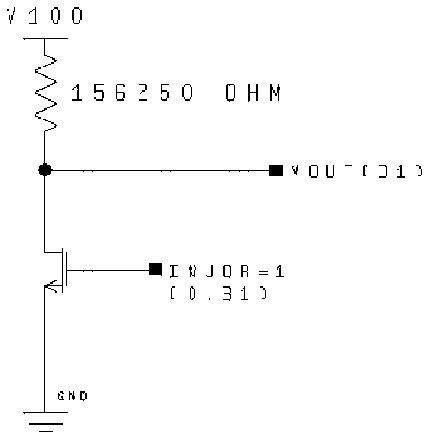


Figure 5-15 Equivalent circuit of the 32 load resistors connected to the pull down transistor of COLINJ(0,31).

Instead of the pull-down transistor being loaded by a 5Mohm resistor, it is loaded with 32 5Mohm resistors in parallel, with an equivalent resistance of 156.250kohm as shown in Figure 5-15. This results in a voltage divider network between the load resistors and the on-resistance of the COLINJ pull-down transistor. In this case, although INJOR is logic high, the transistor may not be able to pull down VOUT(31) close to ground since the load resistance has been reduced significantly. The voltage output during the ground state period will then be an attenuated square wave rather than a voltage close to 0V.

Case 2: Programming a normal phase change

During normal operation of the COL31 cell, the INJ data is set to logic low and the INJOR gate voltage is low, turning off the COL31 pull-down transistor. The resulting circuit at the output is shown in Figure 5-16.

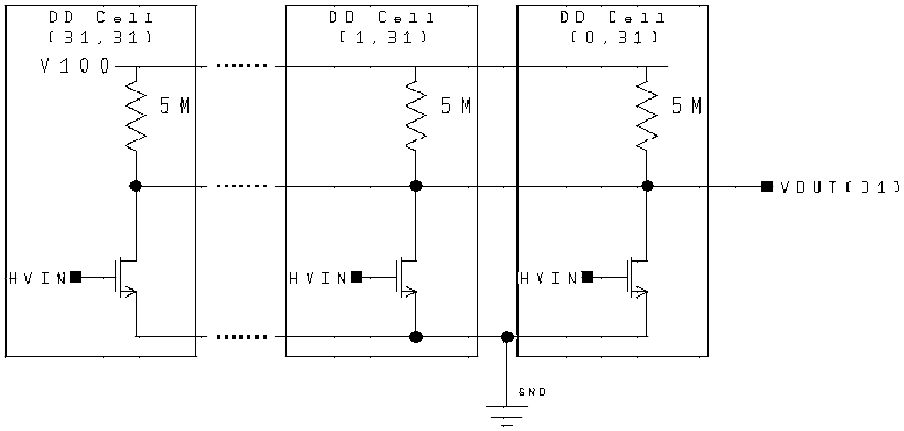


Figure 5-16 Equivalent circuit of the 32 driver cells in COL31 with their outputs connected together and the pull down transistors of COLINJ are all turned off.

Upon reset, the HVIN signals of all the COL31 drivers are equal to VIN and VOUT(31) is 180-degrees in-phase with VIN. If, for example, the digital driver cell at (0,31) is programmed with a logic high phase bit, its HVIN becomes equal to VINB. Therefore, when VIN is high, all the HVIN in COL31 are also high except for (0,31), whose HVIN is low and the output at VOUT(31) is still pulled low by 31 of the 32 digital driver transistors. When VIN is low, all the HVIN in COL31 are also low except for (0,31), whose HVIN is high. This creates the same resistor network found in Case 1 and the equivalent circuit is a single HV NMOS from (0,31) loaded by 32 parallel 5Mohm resistors. Because the equivalent parallel resistances are much less than 5Meg, the single HV NMOS cannot pull the output all the way down to ground and a significant non-zero voltage results.

Finally, the absence of the probe loading effect implies a reduction of the load resistance of the digital driver HV NMOS transistors. Since all 32 loads of COL31 are connected in

parallel, the resulting load is significantly reduced to 156.250kohm and the probe loading effect is not observed.

5.2. Experimental Movement of Fluids by UTMDACC

Fluid droplet movement experiments are performed on PFP1K by UTMDACC and their results are discussed here. The following information is obtained from [2] and is summarized here. In the test, a droplet composed of 180nL of PBS (phosphate buffered saline) with 701um diameter is placed in a suspending medium of 1-bromododecane and moved across the surface of PFP1K coated with ~5 microns of SU-8 topped with a monolayer of FluoroPel 1604 (containing micro vinyl granules ~4 microns across).

The movement of the droplet is controlled by under partial software control driven by the Lynntech Processor Board. PFP1K is operating with a V100=25V, VIN=5Vpp at an operating frequency of f=19Hz. The control sequence of the droplet is performed in four steps:

1. Set the current electrode to secure the droplet
2. Reset the current electrode to release the droplet
3. Set the next electrode to move the droplet between current and next electrode
4. Reset the next electrode to center up the droplet on next electrode

The time lapsed photos of a moving droplet taken from a video are shown in Figure 5-17. In the video, between t=0s (Figure 5-17a) and t=10s (Figure 5-17b), the droplet is moved downward across the array. Following that, the droplet is moved to the right as shown in Figure 5-17c. Then, the droplet is moved upwards across the array as shown in Figure 5-17d. Finally, it is moved slightly to the left as shown in Figure 5-18e.

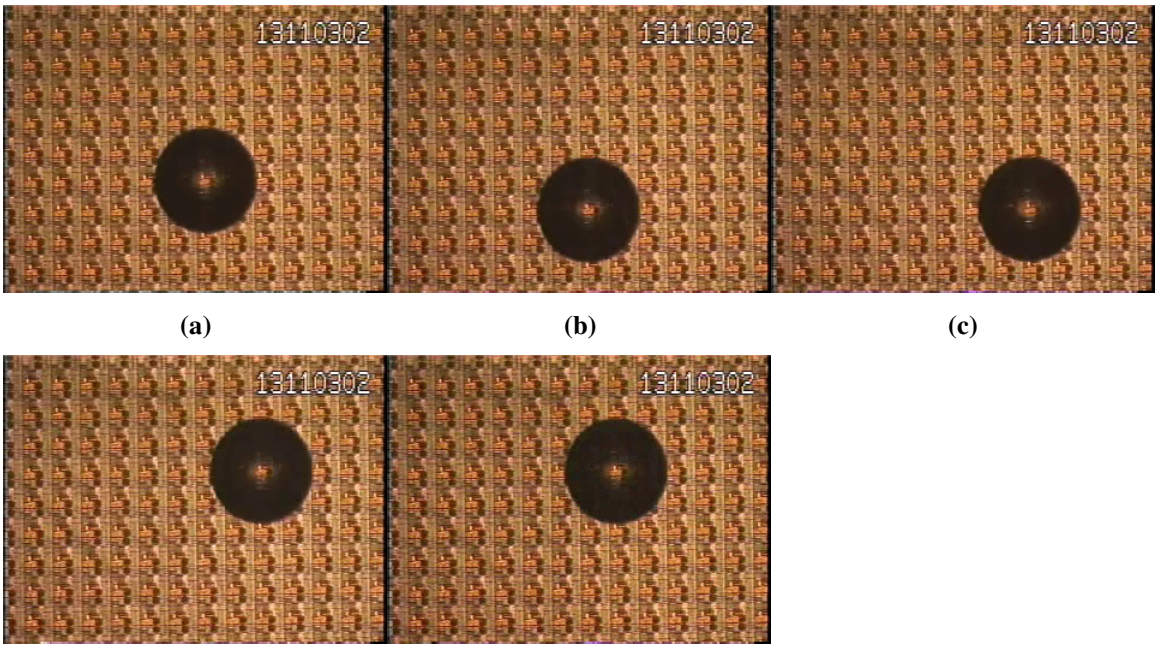


Figure 5-17 Time lapsed photos of the droplet movement video at (a) t=0s (b) t=10s (c) t=42s (d) t=88s (e) t=115s

Discussion

The video shows that the array is capable of moving the droplet in all four directions. One effect observed during this experiment is the stickiness of the droplet to the coated PFP1K surface, which is due to charge build up. The use of a micro-roughened surface may not have been enough to eliminate this charge build-up, which may be a static or mirror charge build-up. Although the oxide layer on top of the chip protects the electrodes from direct contact with the fluid, and thus prevents hydrolysis, it does not prevent charge build up.

In terms of the electrical parameters used in this experiment, a high voltage supply of 25V is used and required to get the droplet moving; much lower than the 100V design specification. Originally a voltage supply of 100V was expected to be required based on

previous tests conducted by UTMDACC and with the expectation that the droplet movement take place in a MEMS chamber mounted atop the chip. Here, however, the droplets are moved across a coated surface of the PFP1K chip and a MEMS structure is not used. If the supply voltage is too high, or greater than 30V, the droplet pulls too hard against the surface and gets stuck against the surface. Also due to the problems of stickiness, a low frequency signal is required to jiggle the droplet out of its secured position. Finally, the long delay between the movements of the droplet is a result of manual programming of the array addresses by the operator.

5.3. Chapter 5 Summary and Conclusions

In this chapter the experiments for the functional verification of PFP1K are described. From tests involving the programming of a standard (non-injection) driver cell, it is shown that the communications circuitry and the driver cell circuitry are functioning correctly. The driver cell has demonstrated its ability to change phase both from a logic high phase data to a logic low phase data as well as from a logic low phase data to a logic high phase data. The simultaneous update feature of the driver cells has also been shown to function properly.

Some of the issues involving the performance of the driver cell such as the peak output level and an early phase output update time have been addressed. The reduction in peak output level to about two-thirds of the supply voltage is due to the probe loading effect of the 10Mohm scope probe and the 5Mohm output resistance of the digital driver. The probe loading effect has been analyzed both through a hand analysis of the scope probe

model as well as through an HSPICE simulation of the digital driver HV NMOS connected to the oscilloscope through the probe. The reduction in the output voltage does not actually exist at the driver output, but only at the oscilloscope input and does not affect the performance of the driver cell circuitry. It is suspected that the premature updating of the output phase is caused by the test setup and exists for V100 greater than about 18V. Despite the presence of the early update time, it was shown that the output update is still controlled by the EN2B signal regardless of the timing.

The injection circuitry is not working correctly due to a layout error connecting all the electrode outputs of COL31 to each other and to all the COLINJ pull down transistors outputs. As a result, the COL31 cells cannot be individually programmed to produce a ground state and also cannot realize a normal phase change operation. The layout error is to be corrected in the next version of the chip, PFP5.

Tests by the UTMDACC on the PFP1K chip show that it is capable of driving the appropriate signals needed to facilitate droplet movement. A droplet is moved across a coated PFP1K chip in all four directions. The signal requirements used during operation are more lenient than expected, requiring a high voltage supply of only 25V at an operating frequency of 19Hz. A major issue affecting the movement of the droplet is the stickiness of the droplet to the surface of the PFP1K chip.

In the next chapter, a summary of the thesis is given and future developments are discussed.

References

[1] Tektronix, "Instruction Manual: P6009 120 MHz 100X Probe," [Accessed 2004 Mar 1], Available at: http://www.tek.com/site/mn/mnfinder_detail/1,1096,,00.html?id=1940&pn=070040102

[2] J. Schwartz, UTMDACC, (email communication), November 14, 2003

Chapter 6 Summary and conclusions

6.1. Summary

In this thesis, the development of a programmable high voltage electrode driver engine for a fluidic processing system employing dielectrophoresis is described. The motivation for the design of the PFP IC comes from its application in a fieldable, microchannel fluidic analysis system. To understand the design specifications and requirements of the PFP IC as a component of the entire system, the fluidic processor as a whole was described in Chapter 2 based on information provided by UTMDACC. In Chapter 2, the concept of dielectrophoresis as the mechanism for fluid droplet transport was explained and the prototype handheld device consisting of the PFP IC, a MEMS chamber for the containment of the fluid droplets and the software interface by PDA was described. High voltage output is required to produce enough DEP force to move the droplets and configurability of the outputs between two phase states is required to create potential differences between electrodes.

To understand the capabilities of the high voltage SOI technology in integrating high and low voltage single-chip systems, the characteristics and design of high voltage transistors are discussed in Chapter 3. Parameters such as the device dimensions, layer thicknesses, doping concentration and biasing contribute to the breakdown voltage of the high voltage devices. Although high voltage NMOS and PMOS transistors have been shown to achieve very breakdown voltages when individually tested, integration with each other and with low voltage CMOS circuits greatly limits the device dimensions, backgate

biasing conditions and therefore reduces their common breakdown voltage in a CMOS circuit. As a result, high voltage CMOS circuits cannot achieve as high a breakdown as their individual transistors when biased and operated independently. Therefore, an NMOS resistor loaded pull-down circuit is used for the final high voltage output driver design, rather than some type of CMOS high voltage level shifter circuit.

The communication and driver circuitry was described in Chapter 4 and their operation was tested in a piecewise fashion. First, the latch used as a building block for the memory elements used in the shift register and the digital driver is described in detail and its cascaded configuration as a dual latch memory cell is described. Following that, the digital driver cell, cell array, communications shift register and decoder circuitry are discussed along with data suppporting their correct operation on PFP1K. The HSPICE design optimization of the data buffers for driving intermediate signals with large fan-outs is described. Finally, the injection circuitry designed to permit a third state at the output of the COL31 driver cells is presented.

Based on tests conducted by UC Davis, it was verified that PFP1K is capable of both array programmability and high voltage operation as described in Chapter 5. The system was tested as a whole and entire programming sequences targeting specific driver cells to demonstrate phase changes were performed. Monitoring phase transitions at the output of the targeted cells through microprobing of the M3 electrodes infers correct operation of the communications circuitry, decoders, data buffers and driver cells.

Several issues evolved from the testing of the high voltage drivers. When probed, the peak driver output voltage was less than the high voltage supply and phase changes in the output seemed to occur before the EN2B signal was pulsed. The reduced peak output was explained through the effect of the probe loading and the large output resistance used at the digital driver output. To investigate the early update of output phase changes at high supply voltages, further tests were conducted to verify control over the electrode array output by the EN2B signal despite monitoring an early update of the output phase. Taking into account the explanation of the anomalous behavior, the digital drivers are capable of 100V operation with phase change capability. An error in the layout rendering the COL31 and COLINJ circuitry inoperable was found and its effect on the outputs of COL31 was explained in detail. In the layout error, the outputs of the COL31 cells were shorted together, preventing both a proper setting of the zero voltage ground state and normal phase switching operation of the COL31 drivers.

Another limitation discovered during testing is the speed of the circuitry. The communications electronics seem to be capable of at least 5kHz operation, but the output drivers, probably due to the large electrode size and its connection to the oscilloscope through the microprobe, protoboard and scope probe cannot operate at the desired 10kHz frequency and was instead tested at 100Hz. However, the low operating frequency may not be a limiting factor in the operation of PFP1K during actual fluid transport since the frequency used in the UTMDACC tests is much less at 19Hz.

Tests conducted by the UTMDACC have shown that the PFP1K is capable of moving droplets across its surface at a 19Hz operating frequency when using a 25V high voltage supply. The conditions under which the droplet movement is tested are different here than originally planned. A MEMS structure is not used to facilitate the droplet movement. Rather, the droplet is transported across the PFP chip surface coated with 5 microns of SU-8. In addition, an effect of droplet stickiness limits the high voltage supply to around 25V. Increasing the high voltage supply beyond 30V will lead to adhesion of the droplet to the coated surface, preventing lateral movement. The ability of PFP1K to provide the required signals to transport perform actual droplet movement further confirms its functionality as well as the conceptual aspects of the programmable fluidics processor as a whole. Also, a low operating frequency of 19Hz was required to loosen the droplet from its resting place and move it to the adjacent electrode. Thus, the operating frequency limitation of the driver cell may be less of an issue than the micro roughened chip surface coating or charge build-up causing this droplet stickiness.

6.2. Further Developments and Research

Another generation of the PFP IC, PFP5, is under development. In PFP5, the COLINJ errors are corrected and a glass MEMS device is planned for use in place of the PDMS MEMS chamber due to reported problems with the PDMS material interacting with the bromododecane medium. The details of the glass structure are still being worked out at this time. Additionally, the drivers in PFP5 feature electrodes of 133um square rather than 100um square as found on PFP1K.

One possible improvement to the PFP1K is the use of a CMOS high voltage driver rather than the resistor loaded HV NMOS. Originally it was assumed that 100V breakdown of the digital driver was required. Since a CMOS high voltage level shifter using the XI10 SOI technology cannot achieve that breakdown, it was not used. However, since UTMDACC has successfully operated the PFP1K with a 25V supply, perhaps the digital driver can be replaced with some type of CMOS high voltage level shifter. A CMOS high voltage driver can then eliminate the static power dissipation of the resistively loaded HV NMOS driver.

One area of further research of the PFP IC is to implement a sensing scheme for droplets present above the electrodes. A sensing scheme would provide feedback into the system and allow bi-directional communication between the PFP system and the controlling board/user. Because the circuitry need be separated from the droplets to prevent hydrolysis, one possible sensing scheme may be based on capacitive coupling of charges between the droplets and the electrodes.

Appendix A: Table of Abbreviations

Table A-1 Table of abbreviations

Abbreviation	Description
AC	Alternating Current
BOX	Buried Oxide
CMOS	Complementary Metal-Oxide-Semiconductor
DC	Direct Current
DEP	Dielectrophoresis
DI	Dielectric Isolation
DL	Dual Latch
HV	High Voltage
IC	Integrated Circuit
JI	Junction Isolation
LLNL	Lawrence Livermore National Laboratory
LOCOS	Local Oxidation of Silicon
MEMS	Micro Electro Mechanical Systems
MESA	Mesa etching
PBS	Phosphate Buffered Saline
PDMS	Polydimethylsiloxane
PFP	Programmable Fluidics Processor
RESURF	Reduced Surface Field
SOI	Silicon-On-Insulator
UCD	University of California, Davis
UTMDACC	University of Texas, MD Andersen Cancer Center
XFAB	X-fab Semiconductor Foundries
XI10	Xfab SOI 1.0um Technology

Appendix B: Test Equipment, Parts and Setup

Table B-1 List of test equipment and testing hardware

Part	Description
HP Digital Oscilloscope 5422A	Oscilloscope used to probe and capture PFP waveforms
Tektronix probes P6009, P6137	Probes used in conjunction with oscilloscope
Tektronix DAS 9100 Series Digital Analysis System	Digital signal generator for PFP control inputs
Tektronix DAS9100 P6452 Data Acquisition Probes 91A32/91A08 (2)	Probes used in conjunction with DAS9100
Micromanipulator Co. HS 6000 probe station	Microscope probing station used to observe and probe PFP electrode outputs
Micromanipulator Model 412 probe holder	Adjustable microprobe holder with magnetic base used to hold Micromanipulator probe
Miscellaneous Micromanipulator probes (2)	Used to probe the chip surface
HP 6205C Dual DC Power Supply	Power supply
Tektronix CP5250 Triple Output Power Supply	Power supply
HP 6216C Power Supply	Power supply
AMP 288-pin ZIF PGA socket	288-pin ZIF PGA socket used for mounting PFP1K and PFP3 adapters
Emulation Technology, Inc. Adapt-a-board socket 80-Qf08Z-P4	Adapter used to convert to PFP3 package to ZIF PGA socket
SYNTAX No. PC-4079 13-B	Test probe card
20 conductor ribbon cable	For routing between the test probe card and a protoboard
20 pin ribbon cable DIP header (10)	Connects ribbon cable to 20 pin header
20 pin DIP socket (9)	Connects 20 pin header to test probe card
Jameco Breadboard JE26	Test protoboard

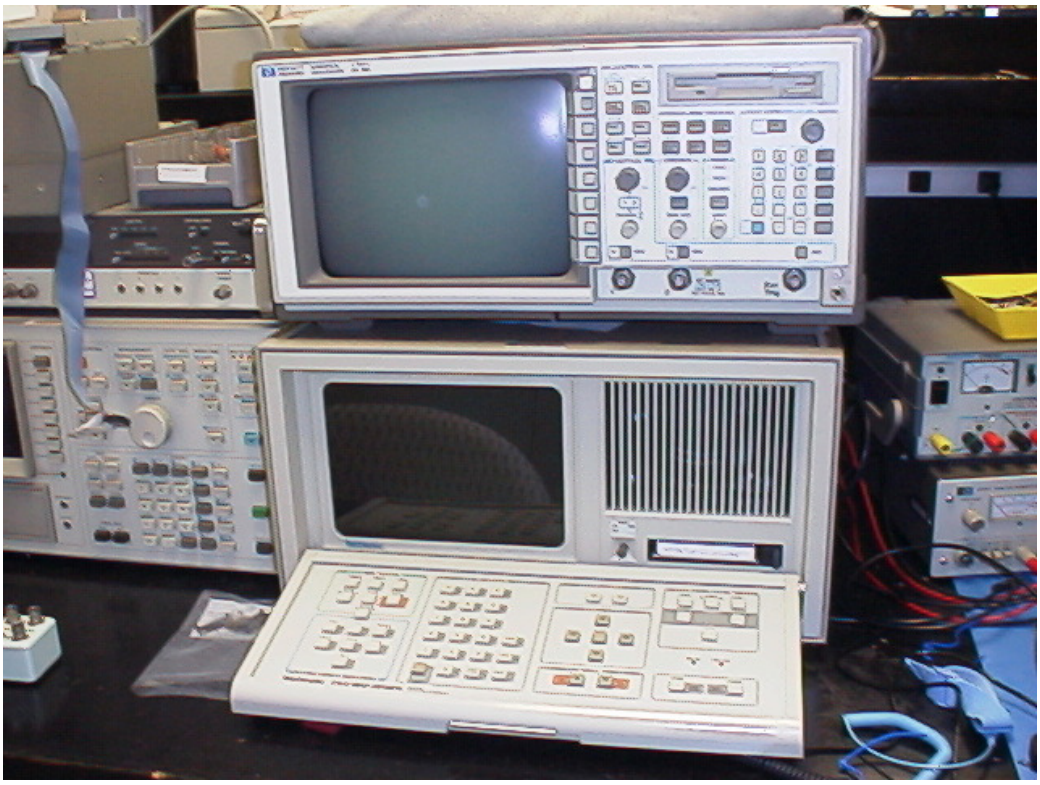


Figure B-1 HP Digital Oscilloscope 5422A and Tektronix DAS 9100 Series Digital Analysis System

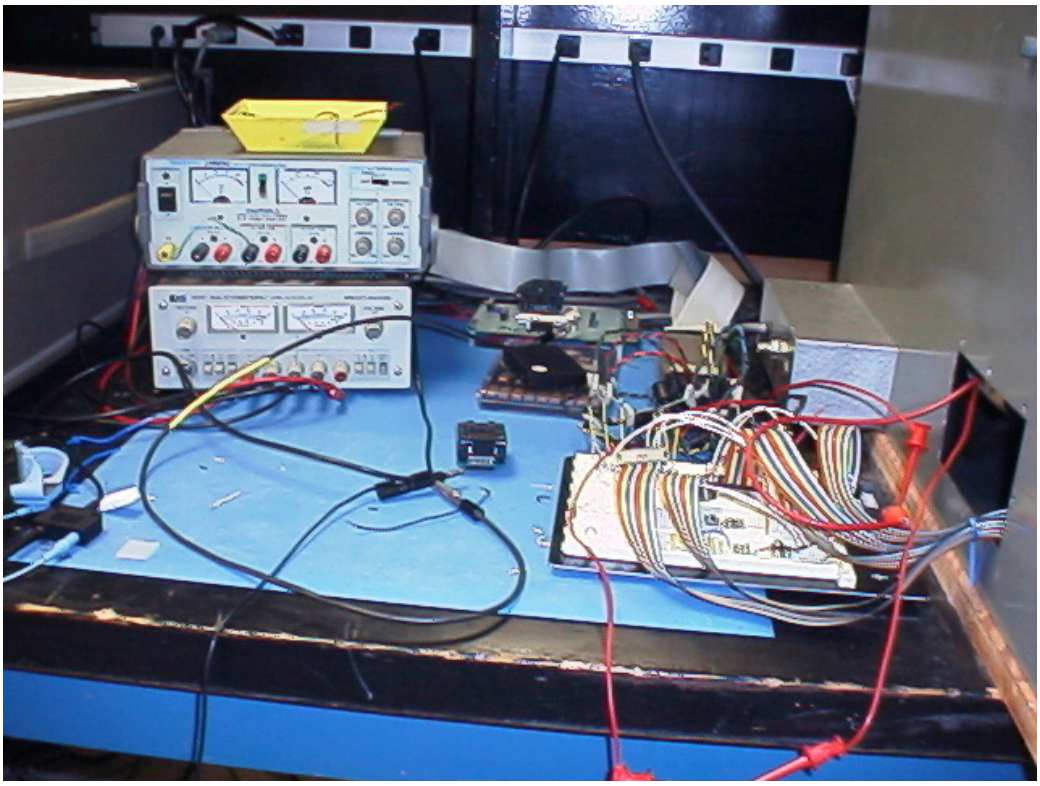


Figure B-2 Power supplies and protoboard for ribbon cable connection

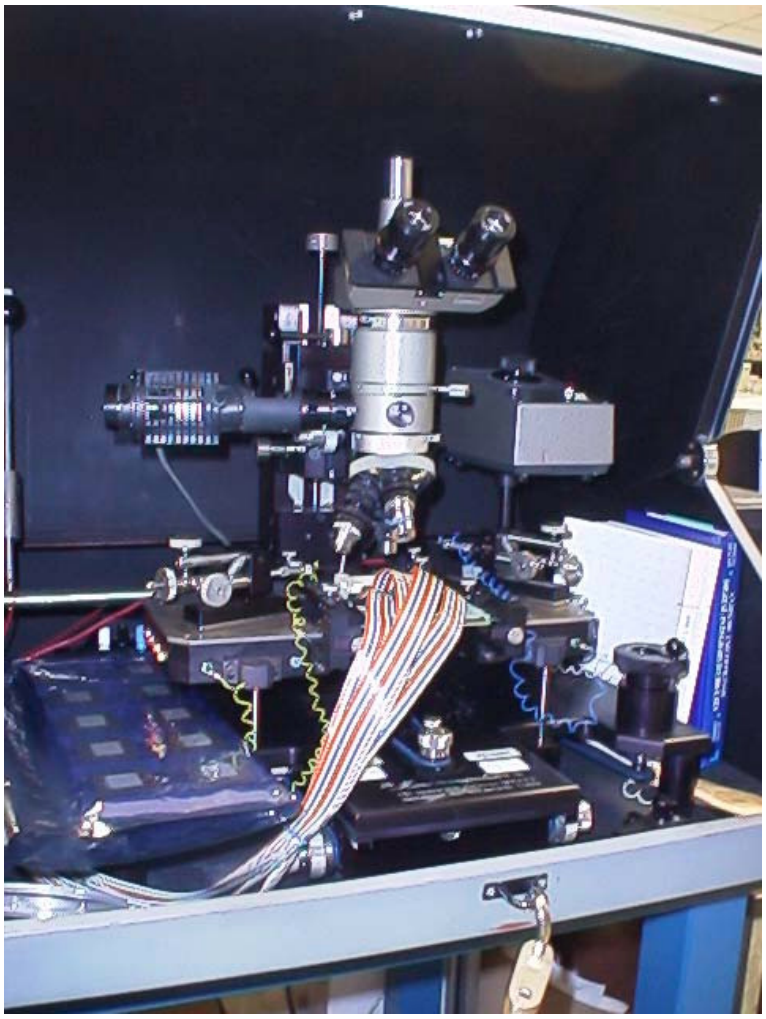


Figure B-3 Micromanipulator Co. HS 6000 probe station with PFP probe card and ribbon cables

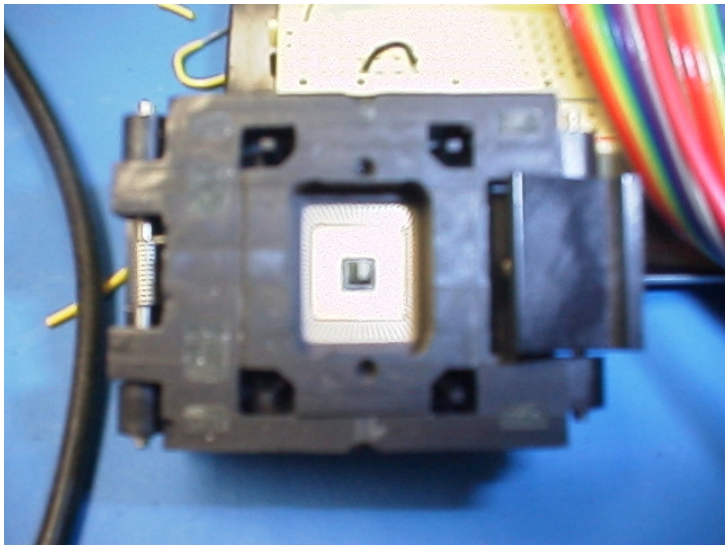


Figure B-4 Adapt-a-board socket 80-Qf08Z-P4 modified to open top for testing of PFP3

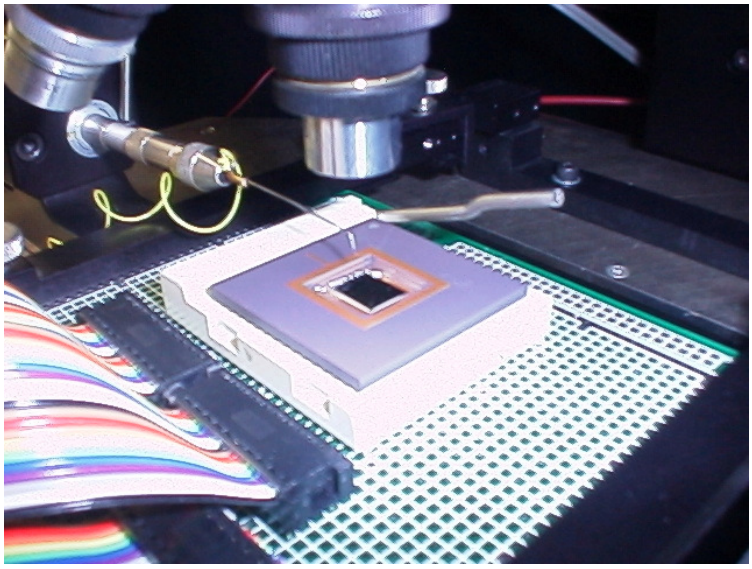


Figure B-5 PFP1K seated in AMP 288-pin ZIF PGA socket and under microscope for testing

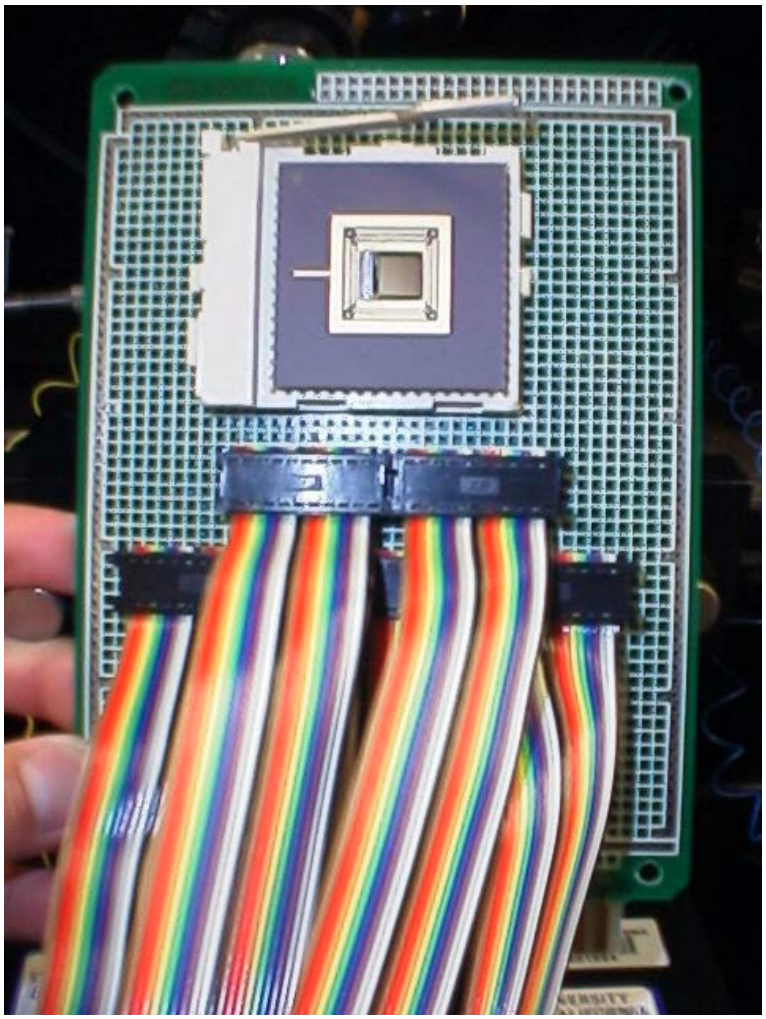


Figure B-6 PFP test probe card using SYNTAX No. PC-4079 13-B

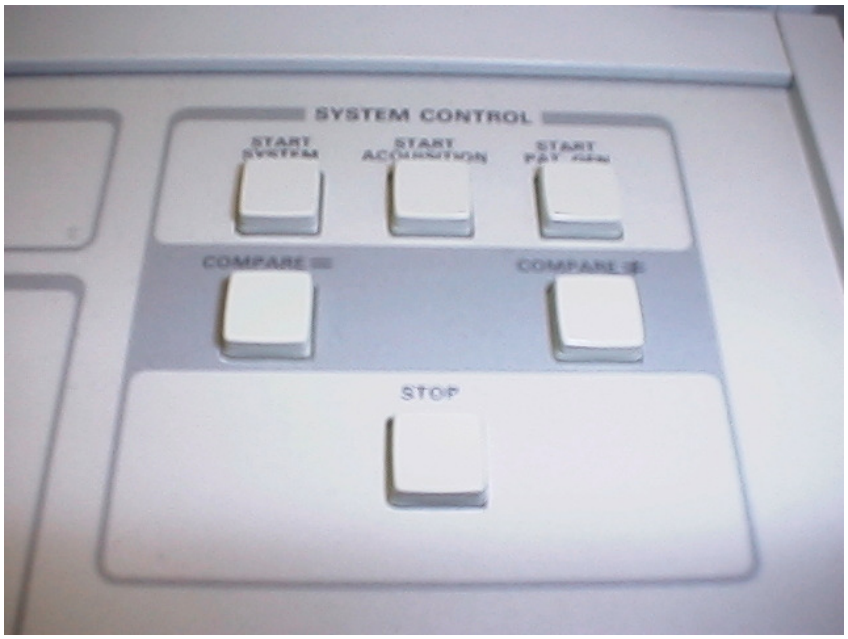


Figure B-7 DAS9100 control keypad